CBCS SCHEME

USN | | | | | | | | | | |

18MT35

Third Semester B.E. Degree Examination, June/July 2025
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. With neat circuit diagram and waveforms. Explain the operation positive and negative shunt dippers with and without bias voltage. **(10 Marks)**

b. Explain the operation of positive and negative clampers. **(10 Marks)**

OR

2 a. Explain the operation of first order lowpass butterworth filter and derive the expression for gain. **(10 Marks)**

b. Explain the operation of wide band pass and Narrow band reject filter. **(10 Marks)**

Module-2

3 a. Explain the operation of phase shift oscillator with circuit diagram and waveform. **(06 Marks)**

b. Design the phase shift oscillator, so that $f_0 = 200$ Hz for $C = 0.1\mu F$. **(04 Marks)**

c. Derive the expression for frequency of oscillation for a wien bridge oscillator. **(10 Marks)**

OR

4 a. Explain the operation of inverting and Non inverting comparators. **(10 Marks)**

b. Explain the operation of inverting comparator as Schmitt trigger with help of waveforms and hysteresis voltage. **(10 Marks)**

Module-3

5 a. Explain the pin diagram and architecture of 555 timer. **(10 Marks)**

b. Explain the operation of 555 timer as monostable multivibrator. **(10 Marks)**

OR

6 a. Explain the operation of 555 timer as Astable multivibrator. **(10 Marks)**

b. Explain the working of astable multivibrator as free running ramp generator. **(10 Marks)**

Module-4

7 a. Simplify the boolean function
$F(w, x, y, z) = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. **(04 Marks)**

b. Explain the full adder with truth table and logic diagram. **(06 Marks)**

c. Explain Quadraple 2 to 1 line multiplexer with function table. **(10 Marks)**

OR

8 a. Construct A 4 × 16 decoder with two 3 × 8 decoders. **(06 Marks)**

b. Design a BCD to decimal decoder. **(10 Marks)**

c. Implement the following function with a multiplexer F(ABCD) = Σ(0, 1, 3, 4, 8, 9, 15). **(04 Marks)**

Module-5

9 a. Explain the operation of clocked RS flip-flop with logic diagram and characteristics table. **(06 Marks)**

b. Explain the operation of clocked T flip-flop with logic diagram and characteristics equation. **(06 Marks)**

c. Explain the operation of Master – slave JK flip-flop. **(08 Marks)**

OR

10 a. Explain the operation of BCD ripple counter with state diagram and logic diagram. **(10 Marks)**

b. Explain the operation of binary 4-bit up down counter. **(10 Marks)**

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