CBCS SCHEME - Make-Up Exam

USN

BMT304

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Describe the connection between memory and processor with the respective registers.	10	L2	CO1
	b.	Discuss in brief different types of keyparameters that affect processor performance.	5	L2	CO1
	c.	Classify big-Endian and Little Endian method with neat diagram.	5	L1	CO1
		OR			
Q.2	a.	Outline the basic instruction types with an example.	10	L2	CO1
	b.	Outline branching concept by considering example of adding n numbers using straight line program and using loop.	10	L2	CO1
		Module – 2			
Q.3	a.	Describe the following addressing nodes with an examples: i) Indirect ii) Indexing iii) Absolute.	10	L2	CO1
	b.	Classify shift and rotate instruction with example.	10	L1	CO1
		OR			
Q.4	a.	Define stack, explain assembly instruction for push operation and pop operation.	10	L2	CO1
	b.	What is assembler directive? Discuss any five assembler directive with an examples.	10	L2	CO1
		Module – 3			
Q.5	a.	Outline the sequence of events involved in handling interrupt request from a single device.	6	L1	CO1
	b.	Describe I/O interface for an input device with necessary diagram.	6	L1	CO1
	c.	Explain a program that reads one line from keyboard stores it in memory buffer and Echos it back to the display.	8	L1	CO1

		OR			
Q.6	a.	Discuss the interrupt nesting. With neat diagram and implementation of interrupt priority using individual interrupt request and acknowledge lines.	10	L2	CO1
	b.	Describe the interrupt priority scheme with a necessary diagram.	10	L2	CO1
		Module – 4			
Q.7	a.	Outline connection of the memory to processor with a neat diagram.	6	L2	CO1
	b.	Develop the organization of 1K × 1 memory chip and explain its working.	8	L2	CO1
	c.	Summarize the various types of ROMs.	6	L1	CO1
		OR			
Q.8	a.	Describe the internal organization of 2m × 8 dynamic memory chip with neat diagram.	10	L2	CO1
	b.	Discuss the working of single transistor dynamic memory cell.	5	L1	CO1
	c.	Briefly explain the secondary storage systems.	5	L1	CO1
		Module – 5			
Q.9	a.	Describe single bus organization of the datapath inside a processor with a necessary diagram.	10	L2	CO2
	b.	Outline control sequence for an unconditional branch instruction.	5	L1	CO1
	c.	Illustrate the action needed to execute instruction MOV (R_1), R_2.	5	L1	CO1
		OR			
Q.10	a.	Describe hardwired control unit organization in a processing unit.	10	L1	CO1
	b.	Discuss any three bus organization of the data path, with a necessary diagram.	10	L1	CO1

* * * * *