CBCS SCHEME - Make-Up Exam

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BEC602

Sixth Semester B.E./B.Tech. Degree Examination, June/July 2025
VLSI Design and Testing

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain CMOS as Logic inverter.	5	L2	CO1
	b.	Draw the schematic diagram of 2-I/P NOR gate and explain the operation.	5	L3	CO1
	c.	Draw the schematic diagram of following Boolean logic: i) $y = \overline{(ABC + D)E}$ ii) $y = \overline{((A + B)\cdot C) + D)}$ iii) $y = \overline{AB + (C + D)}$	10	L3	CO1
		OR			
Q.2	a.	Discuss about types, symbolic representation and physical structure of MOSFET with neat sketches.	8	L2	CO1
	b.	Construct 2-input EXOR gate using transmission gate logic.	6	L3	CO1
	c.	Write the structural representation of 3-input NOR gate.	6	L3	CO1
		Module – 2			
Q.3	a.	Derive the equation for drain current of a MOSFET in non-saturated and saturated region of operations.	8	L2	CO2
	b.	Differentiate PMOS and NMOS transistor.	6	L2	CO2
	c.	What is Latch-up in CMOS inverter? Explain how it can be prevented.	6	L2	CO2
		OR			
Q.4	a.	Explain DC characteristics of CMOS inverter and obtain the relationship for output voltage at different region of DC characteristics.	12	L2	CO2
	b.	Describe the transmission gate logic with neat diagram. Also explain in detail PMOS and NMOS behavior.	8	L2	CO2
		Module – 3			
Q.5	a.	Describe in steps the P-Well process of CMOS technologies with neat sketches.	10	L2	CO3
	b.	Describe Lambda based SOI design rules by appropriate layer representation with dimensions.	10	L2	CO3

		OR			
Q.6	**a.**	Describe the following types of capacitances present in MOS device with relevant equations: i) Parasitic capacitances ii) Diffusion capacitances	**10**	**L2**	**CO3**
	b.	Write short notes on scaling of MOS transistors.	**6**	**L2**	**CO3**
	c.	Explain dynamic power dissipation in CMOS gate.	**4**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Explain the operations of C^2MOS logic and draw the schematic for the function $y = \overline{(A \cdot B + (D + E) \cdot C)}$ using C^2 MOS logic.	**8**	**L3**	**CO4**
	b.	Explain four phase dynamic logic with relevant diagram.	**8**	**L2**	**CO4**
	c.	Draw pseudo NMOS circuit and explain.	**4**	**L2**	**CO4**
		OR			
Q.8	**a.**	Draw schematic representation of CMOS inverter and state its all physical layout considerations and draw its standard layout.	**8**	**L3**	**CO4**
	b.	Explain operations of CVSL logic. State its advantages and disadvantages.	**6**	**L2**	**CO4**
	c.	Write short notes on following I/O structures: i) Input pads ii) Output pads	**6**	**L2**	**CO4**
		Module – 5			
Q.9	**a.**	Explain the behavior of two-inverter basic Bi-stable element.	**10**	**L2**	**CO5**
	b.	Explain the operation of NOR based SR latch circuit and define related lumped load capacitances at output node.	**10**	**L2**	**CO5**
		OR			
Q.10	**a.**	Explain any 4 techniques followed for reduction of complexity of IC design in structured design strategies.	**10**	**L2**	**CO5**
	b.	Write short note on following related automated synthesis: i) Procedural module definition ii) Silicon compiler	**10**	**L2**	**CO5**

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