CBCS SCHEME

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18EC33

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Electronics Devices

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain different types of bonding forces in solids. **(06 Marks)**

b. Consider a semiconductor bar with w = 0.1 mm, t = 10 μm and L = 5 mm for B_z = 10 kg in the direction shown in Fig.Q1(b) and a current of 1 mA. V_{AB} = –2mV, and V_{CD} = 100mV. Find the type of semi-conductor carriers and mobility of the majority carriers. Given 1 kg = 10^{-5} wb/cm^2.

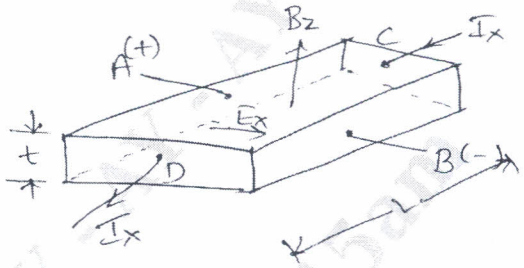

Fig.Q1(b) **(06 Marks)**

c. What are intrinsic and extrinsic materials? Explain briefly by taking suitable example. **(08 Marks)**

OR

2 a. Explain classification of semiconductor, insulator and metals using energy band diagram. **(06 Marks)**

b. A silicon is doped with 10^{17} Arsenic atoms/cm^3. What is the equilibrium hole concentration P_0 at 300°K? Sketch the resulting band diagram showing where is E_F relative to E_i. Assume $n_i^2 = 2.25 \times 10^{20}$. **(06 Marks)**

c. Derive an expression for conductivity and mobility from random thermal motion or electron in solid. **(08 Marks)**

Module-2

3 a. Describe the structure and operation of solar cell. Indicate the significance of fill factor. **(10 Marks)**

b. With a neat diagram, describe in detail avalanche breakdown and derive an approximate analysis of avalanche multiplication. **(10 Marks)**

OR

4 a. Discuss the reverse bias p-n junction indicating the minority carrier distribution and variation of quasifermi levels. **(10 Marks)**

b. Derive an expression for current and voltage for an illuminated junction of photodiode and discuss the operation in various quadrants in I-V characteristic. **(10 Marks)**

Module-3

5 a. Describe the effect of excess hole distribution in cutoff and saturation regime with neat sketch. **(10 Marks)**

b. Explain the switching effect in a common-emitter transistor circuit and specification for switching transistor with neat diagram. **(10 Marks)**

OR

6 a. Describe the schematic representation of p-n-p transistor and summarize the hole and electron flow with proper biasing. **(10 Marks)**

b. Derive the Ebers-Moll equations and represent the coupled-diode equivalent circuit. **(10 Marks)**

Module-4

7 a. Explain the ideal capacitance voltage characteristics of an MOS capacitor with p-type substrate. **(06 Marks)**

b. Illustrate the structure and operation of pn-JFET by varying V_{GS} and V_{DS} independently. **(08 Marks)**

c. List the different types of MOS structures and its symbols. **(06 Marks)**

OR

8 a. Explain the operation of MOS capacitor using energy band diagram for p-type substrate when :

i) Negative gate bias
ii) Moderate positive gate bias
iii) Large positive gate bias. **(08 Marks)**

b. Distinguish between JFET and MOSFET. **(06 Marks)**

c. Describe small signal equivalent circuit of a n-channel pn JFET, with suitable diagram. **(06 Marks)**

Module-5

9 a. List out the different types of IC's along with the advantages and disadvantages and applications of IC's. **(10 Marks)**

b. Describe with neat schematic diagram, Rapid Thermal Processor (RTP) and typical time-temperature profile. **(10 Marks)**

OR

10 a. Explain the fabrication of CMOS twin well process. **(10 Marks)**

b. Describe with neat schematic diagram, optical stepper. **(10 Marks)**

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