CBCS SCHEME - Make-Up Exam

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BEC306C

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Computer Organization and Architecture

ACHARYA INSTITUTE OF TECHNOLOGY :: BANGALORE :: MCA Library Date .....

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the basic operational concept between processor and memory with neat block diagram.	8	L2	CO1
	b.	Summarize single bus architecture with neat diagram.	6	L2	CO1
	c.	Compare Little-endian and Big-endian byte address assignments.	6	L2	CO1
		OR			
Q.2	a.	Explain IEEE standard for single precision and double precision floating point numbers with standard notation.	4	L2	CO1
	b.	Summarize the following with an example. i) Three address instruction ii) Two address instruction iii) One address instruction	6	L2	CO1
	c.	Compare straight line sequencing and branching with suitable example.	10	L2	CO1
		Module – 2			
Q.3	a.	Define addressing mode. Discuss the following addressing mode with example. i) Immediate ii) Register iii) Absolute iv) Index.	10	L1	CO2
	b.	What are Assembler directives? Explain any five assembler directives.	10	L1	CO2
		OR			
Q.4	a.	A two dimensional array having n-rows and four columns. Each row contains the entries for one student and the columns give the ID's and test scores. Develop assembly language program to compute the sum of test scores of all the students in all the tests [3-tests]. Store the corresponding sums in memory.	8	L3	CO2
	b.	Relate the concepts of stacks and Queues.	4	L1	CO2
	c.	Make use of shift and Rotate operations to perform : i) L shiftL # 1, R_0 ii) A shift R # 1, R_0 iii) Rotate R # 1, R_0 iv) Rotate LC # 1, R_0. Consider a register R_0 of size 8-bit with initial data 89H, carry flag is indicated cleared.	8	L3	CO2

		Module – 3			
Q.5	**a.**	Distinguish between memory mapped I/O and standard I/O. Write a program segment to read a line of text from keyboard and display it.	**8**	**L4**	**CO3**
	b.	Outline the concept of Interrupts. Explain various ways of enabling and disabling interrupts.	**8**	**L2**	**CO3**
	c.	Explain interrupt hardware with suitable diagram.	**4**	**L2**	**CO3**
		OR			
Q.6	**a.**	Analyze the following methods of handling interrupts from multiple devices i) Daisy chain method ii) Priority structures	**8**	**L4**	**CO3**
	b.	Explain the following : i) Vectored interrupts ii) Interrupt Nesting.	**4**	**L2**	**CO3**
	c.	Outline DMA controller in a computer system with neat diagram.	**8**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Analyze internal organization of 16 × 8 memory chip with neat diagram.	**8**	**L4**	**CO4**
	b.	Construct a single transistor dynamic memory cell using nMOS.	**6**	**L3**	**CO4**
	c.	With a neat diagram, explain virtual memory organization.	**6**	**L2**	**CO4**
		OR			
Q.8	**a.**	Analyze internal organization of a 2M × 8 dynamic memory chip.	**8**	**L4**	**CO4**
	b.	Explain principle of working of magnetic disk with neat diagram.	**6**	**L2**	**CO4**
	c.	Construct a static RAM cell using two inverter. Explain read and write operation.	**6**	**L3**	**CO4**
		Module – 5			
Q.9	**a.**	Outline single bus organization of datapath inside a processor.	**8**	**L2**	**CO5**
	b.	What are the action required to execute a complete instruction Add (R_3), R_1	**8**	**L1**	**CO5**
	c.	Summarize the organization of Hardwired control unit.	**4**	**L2**	**CO5**
		OR			
Q.10	**a.**	Summarize the basic organization of a microprogrammed control unit.	**4**	**L2**	**CO5**
	b.	Illustrate the organization of the control unit to allow conditional branching in the microprogram with neat diagram.	**8**	**L2**	**CO5**
	c.	Outline Three bus organization of the data path inside a processor.	**8**	**L2**	**CO5**

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