CBCS SCHEME

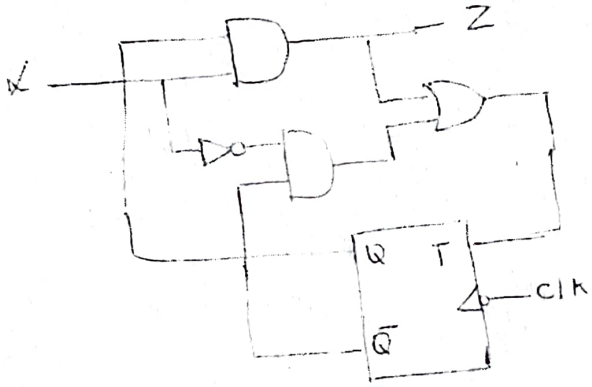
USN | | | | | | | | | | BEE306A

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Digital Logic Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

			M	L	C
		Module – 1			
Q.1	a.	Define combinational Logic with examples.	04	L1	CO1
	b.	Design a combinational logic truth table and circuit diagram so that an output is generated indicating when a majority of four inputs is true.	06	L5	CO1
	c.	Simplify the function using karnaugh map. i) f (A,B,C,D) = Σm (1,3,7,11,15) + Σd (0,2,4) ii) f (A,B,C,D) = ΠM (0, 2, 3, 8, 9,1 2, 13, 15)	10	L4	CO1
		OR			
Q.2	a.	Define the following terms with an example: i) Minterm ii) Maxterm	04	L2	CO1
	b.	Find the prime implicants and essential prime implicants. f(v, w. x,y,z) = Σm (4,5,6,7,9,11,13,15,25,27,29,31)	06	L5	CO1
	c.	Simplify the given Boolean function using Quine Mccluskey method. y = f (a,b,c,d) = Σ (0,1,2,6,7,9,10,12) + d (3,5)	10	L5	CO1
		Module – 2			
Q.3	a.	Explain the design procedure for combinational circuits.	06	L2	CO2
	b.	Implement full subtractor using a decoder and write a truth table.	07	L5	CO2
	c.	Implement the following Boolean function with 8:1 MUX. F(A,B,C,D) = Σm (0,2,6,10,11,12,13) + d (3, 8, 14)	07	L5	CO2
		OR			
Q.4	a.	Design a carry look ahead 4 –bit parallel adder. Show that the time for addition is independent of the length.	08	L5	CO2
	b.	With the help of truth table and simplification using K – map, design a 2 bit comparator using basic gates.	08	L4	CO2
	c.	What is an Encoder? Explain.	04	L1	CO2
		Module – 3			
Q.5	a.	Compare between combinational and sequential circuits.	04	L1	CO3
	b.	With the help of truth table explain application of the SR Latch.	08	L3	CO3
	c.	Derive the characteristics equations of the following flip flops. i) JK flip flop ii) T flip flop	08	L4	CO3

		OR			
Q.6	**a.**	With the help of logic diagram. Explain working of master slave JK Flip Flop along with waveforms. Explain race around condition. How is it eliminated?	**10**	**L2**	**CO3**
	b.	Write the Truth table of SR, T and D flip flops.	**06**	**L4**	**CO3**
	c.	What is the difference between latches and flip flops?	**04**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	With the help of a suitable example, explain the following operations in a shift register i) SISO ii) PISO	**08**	**L4**	**CO4**
	b.	Design mod 6 ripple counter using T – flip flops	**08**	**L5**	**CO4**
	c.	Differentiate between Asynchronous and synchronous counters.	**04**	**L2**	**CO4**
		OR			
Q.8	**a.**	With the help of a diagram, explain ring counter and twisted ring counter.	**06**	**L2**	**CO4**
	b.	Design a synchronous Mod – 6 counter using clocked D Flip Flops.	**08**	**L5**	**CO4**
	c.	Design a 3 bit asynchronous ripple counter using T – flip flops and explain the operation.	**06**	**L5**	**CO4**
		Module – 5			
Q.9	**a.**	Explain Mealy and Moore model of a sequential circuit.	**08**	**L2**	**CO5**
	b.	Construct the transition table, state table and state diagram for the sequential circuit given below. 	**08**	**L5**	**CO5**
	c.	Define state diagram with an example.	**04**	**L2**	**CO5**
		OR			
Q.10	**a.**	With a basic structure, explain clearly programmable Read only Memories (PROMS) and EEPROM.	**10**	**L2**	**CO5**
	b.	Explain the following : i) Flash Memory ii) Read only Memory	**10**	**L2**	**CO5**

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