CBCS SCHEME

USN | | | | | | | | | | 18EE34

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define diode clippers. With circuit diagram and waveforms explain negative shunt clipper. **(06 Marks)**

b. What is transistor biasing? Analyse fixed bias circuit. **(07 Marks)**

c. For the Emitter-bias network of Fig.Q1(c), determine :
i) I_B ii) I_C iii) V_{CE} iv) V_C v) V_E vi) V_B vii) V_{BC}.

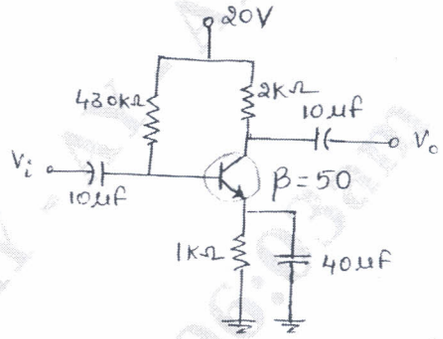

Fig.Q1(c) **(07 Marks)**

OR

2 a. Explain transistor switching action and switching characteristics. **(07 Marks)**

b. State the significance of stability factor and define each. **(05 Marks)**

c. Determine the output voltage for the clamper circuit shown in Fig.Q2(c).

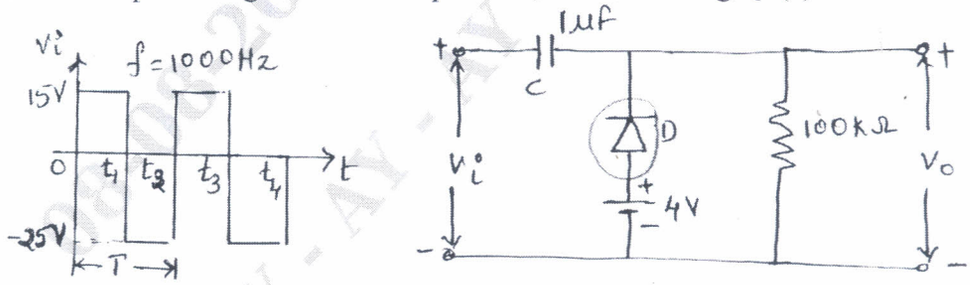

Fig.Q2(c) **(08 Marks)**

Module-2

3 a. For the transistor connected in CE configuration, with voltage divider biasing, determine voltage gain, current gain, input and output resistances using h-parameter model. **(09 Marks)**

b. Explain Miller's theorem. **(05 Marks)**

c. Draw the h-parameter models for all transistor configurations. **(06 Marks)**

OR

4 a. Derive the expression for A_i, A_v and Z_i for an emitter follower circuit using hybrid model. **(10 Marks)**

b. For the network of Fig.Q4(b), determine :
i) Z_i ii) Z_0 iii) A_V iv) A_i.

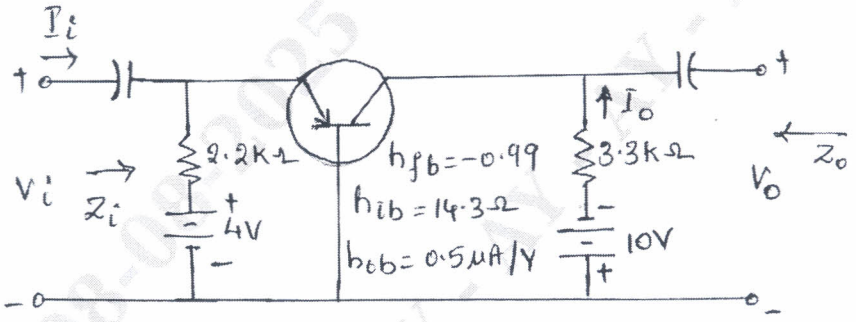

Fig.Q4(b) **(10 Marks)**

Module-3

5 a. State the need for cascading amplifiers. With the block diagram explain two-stage cascaded amplifier. **(10 Marks)**

b. Derive the expression for output resistance for a voltage series feedback amplifier. **(06 Marks)**

c. State the advantages of negative feedback. **(04 Marks)**

OR

6 a. For the Darlington emitter follower circuit, obtain expression for voltage gain, current gain and input impedance. **(10 Marks)**

b. Calculate the voltage gain of the circuit Fig.Q6(b).

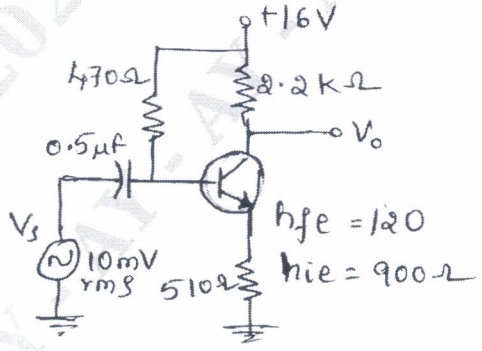

Fig.Q6(b) **(10 Marks)**

Module-4

7 a. Explain the operation of transformer coupled class A power amplifier. Also show that the amplifier has a maximum efficiency of 50%. **(10 Marks)**

b. With the help of neat circuit diagram explain the operation of transistor RC phase shift oscillator. Write the expression for frequency of oscillation. **(10 Marks)**

OR

8 a. With a neat circuit diagram explain the operation of Wein Bridge oscillator. Also derive for frequency of oscillation. **(10 Marks)**

b. How crystal oscillators provide good frequency stability. **(03 Marks)**

c. For a class B amplifier using a supply of V_{CC} = 30V and driving a load of 16Ω, determine the maximum input power, output power and transistor dissipation. **(07 Marks)**

Module-5

9 a. Draw the experimental setup and explain drain characteristics of n-channel JFET with schematic graph. **(10 Marks)**

b. Explain the depletion and enhancement type MOSFETs characteristics. **(10 Marks)**

OR

10 a. Define transconductance g_m and drain resistance r_d of field effect transistor. Explain the procedure to determine them graphically. **(10 Marks)**

b. The fixed bias configuration shown in Fig.Q10(b) with an applied signal V_i had an operating point defined by V_{GSQ} = –2V and I_{DQ} = 5.625 mA with I_{DSS} = 10 mA and V_P = –8 V. The value of Y_{OS} is provided as 40 μs.

i) Determine g_m
ii) Find r_d
iii) Determine Z_i
iv) Calculate Z_0
v) Determine the voltage gain A_V
vi) Determine A_v ignoring the effects of r_d.

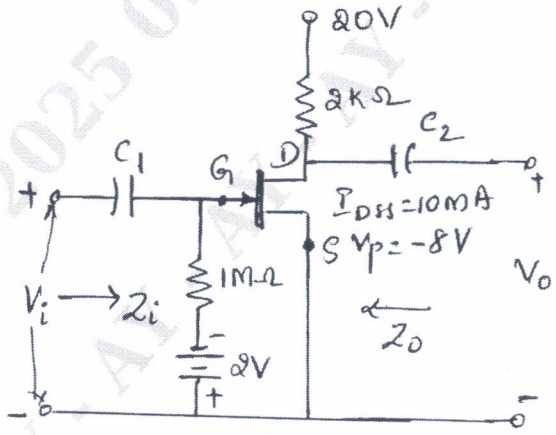

Fig.Q10(b) **(10 Marks)**

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