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BEE306A

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Digital Logic Circuits

Time: hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the definition of combinational logic. Convert the given Boolean expression into minterm canonical form and maxterm canonical form $F(x, y, z) = x + \overline{xz}(y + z)$	8	L2	CO1
	b.	Simplify the function : $y = f(a, b, c, d) = \Sigma m(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$ using Karnaugh map.	6	L2	CO1
	c.	Simplify the function $y = f(a, b, c, d) = \Pi m(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$ using the Karnaugh map.	6	L2	CO1
		OR			
Q.2	a.	Using k-map method, obtain a minimal SOP expression and implement the following function using NAND gate $x = f(a, b, c, d, e) = \Sigma m(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25, 27, 28, 30)$	8	L2	CO1
	b.	Simplify using Quine-McCluskey method and realize the function using a basic gate $M = f(a, b, c, d) = \Sigma m(7, 9, 12, 13, 14, 15) + \Sigma d(4, 11)$	12	L2	CO1
		Module – 2			
Q.3	a.	Design a combinational logic circuit that will convert BCD digit to excess-3 BCD digit using gates. Construct a truth table and simplify each output equation using K-map.	8	L3	CO2
	b.	Implement the following function pairs using 74138IC and gates with minimum numbers of inputs $f_1(a, b, c) = \Sigma m(0, 2, 4)$ $f_2(a, b, c) = \Sigma m(1, 2, 4, 5, 7)$	6	L2	CO2
	c.	Implement a 1-bit comparator using decoder.	6	L2	CO2
		OR			
Q.4	a.	Realize the following Boolean function using 8:1 MUX with 'wyz' as select inputs $v = f(w, x, y, z) = \Sigma m(0, 1, 2, 5, 7, 8, 9, 12, 13)$	5	L2	CO2
	b.	Implement 4 bit parallel adder/subtractor using 4-full address blocks. Explain its operation if $C_{in} = 0$ the circuit should act as adder and if $C_{in} = 1$ the circuit should act as substractor.	5	L2	CO2
	c.	Design a two-bit magnitude comparator with help of the truth table and simplification of the output equation using K-map. Draw the logic diagram.	10	L3	CO2

		Module – 3			
Q.5	a.	What is a Flip Flop? Discuss the working principle of SR flipflop with its truth table. Also highlight the role of SR flip flop in switch de-bouncer circuit.	12	L2	CO2
	b.	Explain the operation of master slave JK flip-flop along with its circuit diagram.	8	L2	CO3
		OR			
Q.6	a.	Obtain the characteristic equation of T, D, SR and JK flip flop.	10	L2	CO3
	b.	Explain the working of master slave SR flip flop with timing diagram.	10	L2	CO3
		Module – 4			
Q.7	a.	Explain the working of 4-bit binary ripple counter using a positive edge trigger T-flip flop with an enable line and relevant timing diagram.	8	L2	CO4
	b.	Design a mod-8 twisted ring counter and explain its operation. Write the count sequence table.	8	L2	CO4
	c.	With a neat logic diagram, explain the operation of 4-bit SISO unidirectional shift register.	4	L2	CO4
		OR			
Q.8	a.	Describe the block diagram of a MOD-7 Johnson counter and explain its operation. Give the count sequence table and the decoding logic used to identify the various states.	10	L2	CO4
	b.	Design a MOD-5 synchronous binary counter using clocked JK flip flop.	10	L2	CO4
		Module – 5			
Q.9	a.	Explain Melay and Moore model in sequential circuit with block diagram and example.	8	L2	CO5
	b.	Design a synchronous circuit using positive edge triggered JK flip flop to generate the following sequence $0 \rightarrow 1 \rightarrow 2 \rightarrow 0$ if input x = 0 and $0 \rightarrow 2 \rightarrow 1 \rightarrow 0$ if input x = 1	12	L3	CO5
		OR			
Q.10	a.	With a basic structure explain clearly Programmable Read Only Memories (PROMS) and EPROM.	13	L2	CO5
	b.	Write short notes on: i) Read only and Read/Write memory ii) Flash memory.	7	L2	CO5

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