CBCS SCHEME

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18EE35

Third Semester B.E./B.Tech. Degree Examination, June/July 2025
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the definition of combinational logic. Convert the given Boolean expression into minterm canonical form and maxterm canonical form :
$F(x, y, z) = x + x'z'(y + z)$. **(08 Marks)**

b. Simplify the function :
$Y = f(a, b, c, d) = \Sigma m(2,3,4,5,13,15) + \Sigma d(8,9,10,11)$ using Karnaugh map. **(06 Marks)**

c. Simplify the function :
$Y = f(a, b, c, d) = \Pi M(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$ using Karnaugh map. **(06 Marks)**

OR

2 a. Convert the following Boolean function into their proper canonical form in decimal notation. i) $f = a'b + bc$ ii) $f = (x' + y)(y + z')$. **(08 Marks)**

b. Simplify using Quine-McCluskey minimization technique for the following function : $f(w, x, y, z) = \Sigma(0, 1, 4, 5, 9, 11, 13, 15)$. **(12 Marks)**

Module-2

3 a. Implement the following using 8 to 1 MUX with a, b and c as select lines.
$f(a, b, c, d) = \Sigma(0,1, 5, 6, 7, 9, 10, 15)$. **(08 Marks)**

b. Implement a 1 – bit comparator using 2 : 4 decoder 74139. **(04 Marks)**

c. Design a priority encoder for a system with the three inputs, with the middle bit with highest priority encoding to 10, the MSB with the next priority encoding to 11, while the LSB with least priority encoding to 01. **(08 Marks)**

OR

4 a. What is carry look ahead adder? Explain general organization of it. **(08 Marks)**

b. Design a combinational circuit that will multiply two 2-bit numbers. **(12 Marks)**

Module-3

5 a. With a neat diagram, explain the working of master-slave JK flip-flop along with waveforms. **(10 Marks)**

b. Explain switch debouncer using SR latch with waveform. **(10 Marks)**

OR

6 a. Write the characteristic equation of SR, JK, D and T flip-flops. **(08 Marks)**

b. Differentiate sequential logic circuit and combinational logic circuit. **(04 Marks)**

c. Explain the operation of SR latch with an example. **(08 Marks)**

Module-4

7 a. Explain with suitable logic and timing diagram :

i) Serial-in serial-out shift register

ii) Parallel-in parallel-out shift register. **(10 Marks)**

b. Compare resisters and counters. Explain the working of 4-bit Asynchronous counter using JK-flip-flops. **(10 Marks)**

OR

8 a. Describe the block diagram of a MOD-7 Johnson counter and explain its operation. Give the count sequence table and the decoding logic used to identify the various states. **(10 Marks)**

b. Design a MOD-5 synchronous binary counter using JK-flip-flops. **(10 Marks)**

Module-5

9 a. Explain Mealy and Moore model in a sequential circuit analysis. **(08 Marks)**

b. Design a sequential circuit using D-flip-flop for the state diagram shown below in Fig.Q9(b).

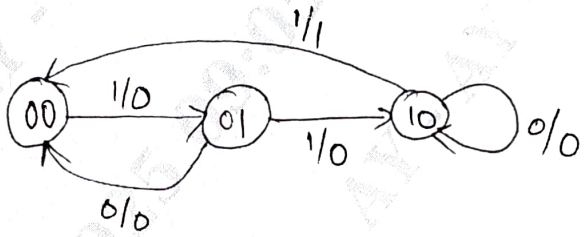

Fig.Q9(b) **(12 Marks)**

OR

10 a. With a basic structure, explain clearly Programmable Read Only Memories (PROMS) and EPROM. **(13 Marks)**

b. Write short notes on :

i) Read only and Read/Write memories

ii) Flash memory. **(07 Marks)**

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