CBCS SCHEME - Make-Up Exam

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BCS402

Fourth Semester B.E/B.Tech. Degree Examination, June/July 2025
Microcontrollers

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, choosing ONE full question from each module.*
M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
1	a.	Differentiate between RISC and CISC processors.	4	L2	CO1
	b.	Explain ARM core data flow model with neat diagram.	8	L2	CO1
	c.	Explain different processor modes provided by ARM7.	8	L2	CO1
		OR			
2	a.	Explain the architecture of a typical embedded device based in ARM core, with a neat diagram.	8	L2	CO1
	b.	Explain the various fields in the current program status register with a neat layout.	6	L2	CO1
	c.	What is pipeline in ARM? Explain the different pipeline stages of ARM9 processor.	6	L2	CO1
		Module – 2			
3	a.	Discuss the load-store instruction with respect to, (i) Single Register Transfer (ii) Multiple Register Transfer	8	L2	CO2
	b.	Explain different arithmetic instructions in ARM processor with an example.	8	L2	CO2
	c.	Explain the multiply instructions of ARM processor.	4	L2	CO2
		OR			
4	a.	Write a ALP to find the Sum of first 10 integer numbers.	6	L3	CO2
	b.	Explain the ARM single-Register and Multiple-Register load-store addressing modes with example.	8	L2	CO2
	c.	Explain the different branch instructions of ARM processor.	6	L2	CO2

		Module – 3			
5	a.	Write a program in C for ARM microcontroller to find factorial of a number.	6	L3	CO3
	b.	Explain why we should avoid using char data type for local variables, with suitable example.	8	L3	CO3
	c.	List and explain different portability issues.	6	L2	CO3
		OR			
6	a.	Discuss how registers are allocated to optimize the program.	6	L3	CO3
	b.	Explain the concept of Loop unrolling with suitable example.	6	L3	CO3
	c.	Explain four register rule used in function calls and also explain the benefits of using a structure pointer in code taking a suitable example.	8	L3	CO3
		Module – 4			
7	a.	With a neat diagram, explain ARM processor exceptions and modes.	10	L2	CO4
	b.	Explain assigning interrupts and interrupt latency.	10	L2	CO4
		OR			
8	a.	Briefly explain what happens when an IRQ and FIQ exception is raised, with an ARM processor.	10	L2	CO4
	b.	Explain firmware execution flow and explain Red Hat Red Boot.	10	L2	CO4
		Module – 5			
9	a.	Explain the basic architecture of cache memory.	10	L2	CO5
	b.	Explain how main memory maps to a cache memory.	5	L2	CO5
	c.	Explain the basic operation of a cache controller.	5	L2	CO5
		OR			
10	a.	Briefly explain Cache line replacement policies.	8	L2	CO5
	b.	Explain briefly the allocation policy on a Cache Miss.	6	L2	CO5
	c.	Explain the following : (i) Write Buffers (ii) Measuring Cache efficiency (iii) Write policy	6	L2	CO5

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