CBCS SCHEME

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21CS643

Sixth Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Advanced Computer Architecture

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Describe the Flyn's classification of computer architectures. **(10 Marks)**

b. Explain the PRAM model and the four variants of the PRAM model. **(07 Marks)**

c. Write a note on the three application models of parallel computers with a neat diagram. **(03 Marks)**

OR

2 a. Describe the types of data dependence and draw the dependence graph showing data and resource dependence using Bernstein's conditions for the following five statements:

P1 : C = D × E
P2 : M = G + C
P3 : A = B + C
P4 : C = L + M
P5 : F = G ÷ E **(08 Marks)**

b. Explain the 16 × 16 baseline network with a neat diagram. **(08 Marks)**

c. Describe the four characteristics in the scalability of parallel algorithms. **(04 Marks)**

Module-2

3 a. Describe the typical VAX 8600 processor CISC architecture. **(07 Marks)**

b. Distinguish between CISC and RISC processors. **(05 Marks)**

c. Describe the VLIW architecture and VLIW execution with degree m = 3. **(08 Marks)**

OR

4 a. Describe the inclusion property and data transfers between the adjacent levels of a memory hierarchy. **(07 Marks)**

b. Describe the Hit Ratio, effective Access Time and hierarchy optimization. **(08 Marks)**

c. Explain the concepts of primary virtual memory and shared virtual memory. **(05 Marks)**

Module-3

5 a. Describe the synchronous and asynchronous bus timing with neat diagrams. **(08 Marks)**

b. Describe the direct mapping cache organization with the neat diagram. **(07 Marks)**

c. Explain the two models of linear pipeline units and the reservation table. **(05 Marks)**

OR

6 a. What is memory interleaving? Discuss the low-order m-way interleaving. **(08 Marks)**

b. Describe the concepts of swapping out and swapping in a process consisting of five resident pages of 0, 1K, 16K, 17K and 55K. **(07 Marks)**

c. Discuss the dynamic non-linear pipeline processors with three stage pipeline and the reservation table for the function x and y. **(05 Marks)**

Module-4

7 a. Discuss the design of cross point switches in a cross bar network. **(08 Marks)**

b. Discuss the concepts of write-through caches protocol of write-invalidate snoopy protocols. **(07 Marks)**

c. Explain the processor consistency for the distributed shared memory. **(05 Marks)**

OR

8 a. Describe the S-Access memory organization in a vector computer. **(10 Marks)**

b. Explain the Fujitsu VP2000 series supercomputer architecture with a neat diagram. **(10 Marks)**

Module-5

9 a. Discuss the OOP model (object oriented programming) in parallel programming. **(10 Marks)**

b. Explain the phases of parallelizing compiler in the modern parallel programming computers. **(10 Marks)**

OR

10 a. Describe the design of a typical processor with a reorder buffer and also with the reservation stations in the functional units. **(10 Marks)**

b. Discuss the concept of operand forwarding in the instruction level parallelism of the superscalar processors. **(10 Marks)**

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