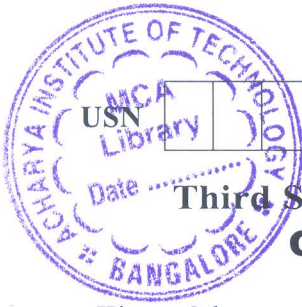


# CBCS SCHEME



BMT304

Third Semester B.E./B.Tech Degree Examination, June/July 2024  
**Computer Organization and Architecture**

Time: 3 hrs.

Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.  
2. M : Marks , L: Bloom's level , C: Course outcomes.

Module – 1			M	L	C
Q.1	a.	Explain the fundamental units of a computer.	10	L2	CO1
	b.	Explain single bus and multiple bus structure.	10	L2	CO1
OR					
Q.2	a.	Differentiate RISC and CISC architecture.	10	L1	CO1
	b.	Explain Big Endian and little Endian assignment.	10	L1	CO1
Module – 2					
Q.3	a.	Explain any 5 addressing mode with example.	10	L2	CO1
	b.	Explain assembler directives.	10	L2	CO1
OR					
Q.4	a.	Explain auto increment and auto decrement mode.	10	L2	CO2
	b.	Explain logical shift and rotate instruction with example.	10	L2	CO2
Module – 3					
Q.5	a.	Explain memory mapped I/o and I/o mapped I/O.	10	L2	CO2
	b.	Explain mechanisms used for interfacing I/O devices.	10	L2	CO2
OR					
Q.6	a.	Explain Direct Memory Access (DMA).	10	L2	CO2
	b.	Explain polling.	10	L2	CO2
Module – 4					
Q.7	a.	Explain the types of ROM.	10	L2	CO3
	b.	Explain cache memory.	10	L2	CO3
OR					
Q.8	a.	Explain static RAM.	10	L2	CO3
	b.	Explain asynchronous DRAM.	10	L2	CO3

## Module – 5

Q.9	a.	Explain single Bus organization.	10	L2	CO3
	b.	Explain register transfer.	10	L2	CO3
OR					
Q.10	a.	Explain connection and control signal for register MDR.	10	L2	CO4
	b.	Explain hardwired control.	10	L2	CO4

\*\*\*\*\*