CBCS SCHEME

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BMT304

Third Semester B.E./B.Tech. Degree Supplementary Examination, June/July 2024

Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain with blockdiagram basic functional units of a computer.	08	L2	CO1
	b.	Write the basic performance equation. Explain the role of each of the parameter in the equation.	05	L2	CO1
	c.	Explain Big-endian and Little-endian method with neat diagram.	07	L2	CO1
		OR			
Q.2	a.	Draw and explain the connection between memory and processor with the respective registers.	08	L2	CO1
	b.	What is straight line sequencing? Explain with example program.	05	L2	CO1
	c.	Write a program that can evaluate the expression $A \times B + C \times D$ in a single accumulator processor. Assume that the processor has load, store, multiply, and add instruction and that all values fit in the accumulator.	07	L2	CO1
		Module – 2			
Q.3	a.	Explain various addressing modes with example.	08	L2	CO2
	b.	What is parameter passing? How are parameters passing? How are parameters passed to sub routine using registers?	06	L2	CO2
	c.	Explain the assembler directives concept with example program.	06	L2	CO2
		OR			
Q.4	a.	Explain logical shift and rotate operations with examples.	08	L2	CO2
	b.	What is stack? Write a routine for safe push operation and safe pop operation.	06	L1	CO2
	c.	Find the effective address of the memory operand in each of the following instruction: @Load 20(R_1), R_5 @Move #3000, R_5 @Add – (R_2), R_5 where $R_1 = 1200$ and $R_2 = 4600$	06	L3	CO2
		Module – 3			
Q.5	a.	What is memory mapped I/O? Explain I/O interface for an input device with a neat diagram.	06	L1	CO2
	b.	Discuss the different schemes available to enable and disable interrupts.	06	L1	CO2
	c.	What is interrupt nesting? Explain with a neat diagram, the implementation of interrupt priority using individual interrupt request and acknowledge lines.	08	L1	CO2
		OR			
Q.6	a.	What is DMA? With a neat diagram, discuss how DMA controller registers accessed by the processor to initiate transfer operations.	08	L1	CO2
	b.	Explain how simultaneous interrupt request from several I/O devices will be handled by a processor through a single INTR line.	06	L2	CO2
	c.	Define bus arbitration. Explain centralized bus arbitration.	06	L1	CO2

		Module – 4			
Q.7	**a.**	Explain the organization of 16 × 8 memory chip.	**10**	**L2**	**CO3**
	b.	Define ROM. List and explain various types of ROMs.	**10**	**L1**	**CO3**
		OR			
Q.8	**a.**	What is virtual memory? Explain virtual memory organization with a neat diagram.	**10**	**L2**	**CO3**
	b.	Explain the internal organization of a 2M × 8 asynchronous DRAM chip.	**10**	**L2**	**CO3**
		Module – 5			
Q.9	**a.**	Draw the diagram of single bus organization of the data path inside a processor and explain the steps to execute an instruction.	**10**	**L2**	**CO3**
	b.	Explain the hardwired control unit organization in a processing unit.	**10**	**L2**	**CO3**
		OR			
Q.10	**a.**	Explain the micro-programmed control unit organization in a processing unit.	**10**	**L2**	**CO3**
	b.	Draw and explain multiple bus organization.	**10**	**L2**	**CO3**

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