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18MT36

Third Semester B.E. Degree Examination, June/July 2024
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Draw the connective between the processor and memory and explain the function s of the following processor registers MAR, MDR IP and IR. **(10 Marks)**

b. Write the basic performance equation and explain with respect to performance of a computer. **(05 Marks)**

c. What is performance measurement? Explain the overall SPEC rating for the computer is a program unit. **(05 Marks)**

OR

2 a. Explain big endian and little endian and draw memory layout of 32 bit integer : abcdef12in hexadecimal how it get stored in big endian and litter endian. **(10 Marks)**

b. Mention four types of operation to be performed by instruction in a computer. Explain with basic types of instruction formats to carryout C ← [A] + [B]. **(10 Marks)**

Module-2

3 a. Explain all the addressing modes in detail. **(10 Marks)**

b. Define assembler directive. List and explain assembler directives. **(10 Marks)**

OR

4 a. Explain the Bus connection for processor keyboard and display. **(06 Marks)**

b. Define stack and queue. Explain routine for a safe pop operation and routine for safe PUSH operation. **(08 Marks)**

c. Explain in detail shift instruction. **(06 Marks)**

Module-3

5 a. With diagram explain the difference between memory mapped I/O and I/O mapped I/O. **(06 Marks)**

b. Write a program that reads one line from keyboard until a newline is encountered and store it is memory buffer and echo it back to display. **(08 Marks)**

c. Explain different methods of handling interrupt latency in various processor architecture. **(06 Marks)**

OR

6 a. Explain interrupt priority scheme (daisy chain) with neat diagram. **(06 Marks)**

b. Explain with neat diagram arrangement of priority groups. **(06 Marks)**

c. Explain in detail the use of DMA controller in a computer system. **(08 Marks)**

Module-4

7 a. Differentiate between SRAM and DRAM. **(04 Marks)**

b. Explain different types of ROM with short description. **(08 Marks)**

c. Discuss the internal organization of a 2M×8 asynchronous DRAM chip. **(08 Marks)**

OR

8 a. Explain memory hierarchy with neat diagram. **(04 Marks)**
b. Explain virtual memory organization. **(04 Marks)**
c. Explain 3 types of mapping functions. **(12 Marks)**

Module-5

9 a. Explain with neat diagram single bus organization of the datapath inside a processor. **(10 Marks)**
b. Write control sequence for execution of the instruction Add (R_3), R_1. **(10 Marks)**

OR

10 a. Explain with neat diagram multiple bus organization. **(10 Marks)**
b. Explain branching instruction along with control sequence for an unconditional branch instruction. **(10 Marks)**

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