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18EC753

Seventh Semester B.E. Degree Examination, June/July 2024
ARM Embedded Systems

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Compare between VLSI and Embedded Systems. (05 Marks)
  b. With a neat diagram, explain the architecture of ARM Cortex-M3 microcontroller. (10 Marks)
  c. Explain briefly Register Organization of Cortex-M3. (05 Marks)

OR

2 a. Define Embedded System. Explain classification of Embedded Systems. (06 Marks)
  b. Compare between push and pop operations. (06 Marks)
  c. Explain briefly:
    (i) AMBA Bus protocol   (ii) Memory
    (iii) Peripherals   (iv) ARM Bus technology (08 Marks)

Module-2

3 a. Explain the following instruction with examples:
    (i) ASR   (ii) LSL   (iii) ROR   (iv) REV (10 Marks)
  b. With a diagram, explain the organization of CMSIS and its benefits. (05 Marks)
  c. Write a note on barrier instruction in Cortex-M3. (05 Marks)

OR

4 a. Explain briefly classification of instructions. (10 Marks)
  b. Explain briefly semihosting overview. (05 Marks)
  c. What are the features of 32-bit ARM state instructions? (05 Marks)

Module-3

5 a. With diagram, explain Thumb-2 technology and instruction set architecture. (10 Marks)
  b. Compare between ARM versus Thumb programmer's models. (05 Marks)
  c. Explain briefly instruction pipeline. (05 Marks)

OR

6 a. Explain briefly branch instructions. (05 Marks)
  b. Explain briefly:
    (i) Data processing instructions
    (ii) Data movement (05 Marks)
  c. Explain briefly barrel shifter with classification. (10 Marks)

Module-4

7 a. Explain the following instructions with example:
    (i) LDMIA   (ii) LDRB   (iii) LDRH   (iv) LDSB   (v) MVN (10 Marks)
  b. Explain with diagram Thumb-2 ARM instruction mapping. (05 Marks)
  c. List and explain the Thumb Application. (05 Marks)

OR

8   a. Explain briefly:
    (i)   C compiler and optimization
    (ii) Basic data types
    (iii) Local variable types   **(10 Marks)**
   b. Explain briefly:
    (i)   Exception handling ARM processor
    (ii) Vector table
    (iii) Link Register Offset   **(10 Marks)**

Module-5

9   a. Explain briefly:
    (i)   Firmware Boot Loader
    (ii) Operating system
    (iii) Memory management units   **(10 Marks)**
   b. Explain briefly:
    (i)   Cache memory
    (ii) Memory hierarchy
    (iii) Embedded system components   **(10 Marks)**

OR

10   a. Explain with basic block diagram of basic architecture of caches memory. **(10 Marks)**
   b. Compare between cache and main memory. **(05 Marks)**
   c. Explain basic operation of cache controller. **(05 Marks)**

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