CBCS SCHEME

USN | | | | | | | | | | |

21EE42

Fourth Semester B.E. Degree Examination, June/July 2024
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Obtain a minimal SOP expression for the function f(a, b, c, d,e) = Σm(3, 7, 11, 12, 13, 14, 15, 16, 18) + d(24, 25, 26, 27, 28, 29, 30, 31) using Karnaugh map method. **(08 Marks)**

b. Design a combinational logic circuit to output the 2's complement of a 4-but binary number
   i) Construct the truth table
   ii) Simplify each output function using K-map and write reduced equations and draw the resulting logic diagram. **(12 Marks)**

OR

2 a. Find a minimal sum for the following Boolean function using Quine – Mc Cluskey method and prime implicant table reduction f(a, b, c, d) = Σ(3, 4, 5, 7, 10, 12, 14, 15) + ϕ(2). **(12 Marks)**

b. Obtain the minimal sum using K-map for the following function
f(a, b, c, d) = Σm(1, 2, 3, 5, 6, 7, 11, 12, 13 14, 15). Find all the prime implicants and essential prime implicants. Draw the logic diagram. **(08 Marks)**

Module-2

3 a. Implement full subtractor using a decoder and write the truth table. **(06 Marks)**

b. Design even parity generator circuit for 4 bit I/P using multiplexer. **(08 Marks)**

c. Write a note on 4-bit priority encoder. **(06 Marks)**

OR

4 a. Design a 2-bit comparator using gates. **(10 Marks)**

b. Explain how a full subtractor can be realized using two half subtractor and OR-Gate. **(10 Marks)**

Module-3

5 a. Draw the logic symbol of the edge triggered JK flip-flop. Obtain its characteristics equations and draw the timing diagram. **(08 Marks)**

b. Explain different types of triggering mechanism employed in flip-flops. **(06 Marks)**

c. Draw the logic circuit of D latch using only NAND gates and explain its operation. **(06 Marks)**

OR

6 a. Explain how T-flip-flop can be converted into SR flipflop. **(07 Marks)**

b. Write the truth table for the following circuit and show that it acts as a T-flip-flop.

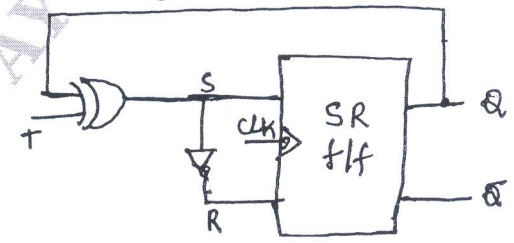

Fig Q6(b) **(07 Marks)**

c. Distinguish between i) Synchronous and Asynchronous circuits ii) Combinational and sequential circuits. **(06 Marks)**

Module-4

7 a. Design a synchronous counter with sequence 0, 1, 3, 7, 6, 4, 0 using JK flip flop. **(08 Marks)**
b. Design a 4-bit binary ripple up counter using negative edge triggered JK f/f. **(04 Marks)**
c. List the steps involved in the design of asynchronous counter. **(08 Marks)**

OR

8 a. Draw a 4 bit Johnson counter, its truth table and timing diagram. Explain its operation. **(08 Marks)**
b. Explain the operation of 4-bit bidirectional shift register. **(08 Marks)**
c. List the applications of shift registers. **(04 Marks)**

Module-5

9 a. Distinguish between Mealy and Moore model with necessary block diagram. **(08 Marks)**
b. Analyze the synchronous circuit of the figure shown Q9(b) i) Write the excitation and output function ii) Form the excitation and state tables.

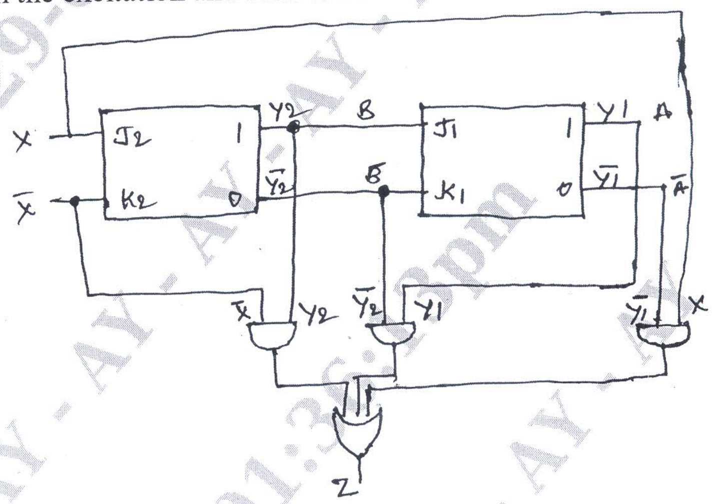

Fig Q9(b) **(12 Marks)**

OR

10 a. Obtain the transition table for the state diagram shown below Fig Q10(a) and design a sequential circuit using JK flip-flop.

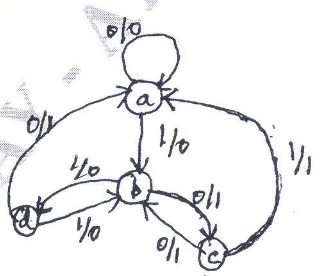

Fig Q10(a) State diagram **(08 Marks)**

b. Explain the classification of semiconductor memories. **(04 Marks)**
c. Discuss the following types of ROM memory i) EPROM ii) PROM iii) EEPROM. **(08 Marks)**

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