CBCS SCHEME

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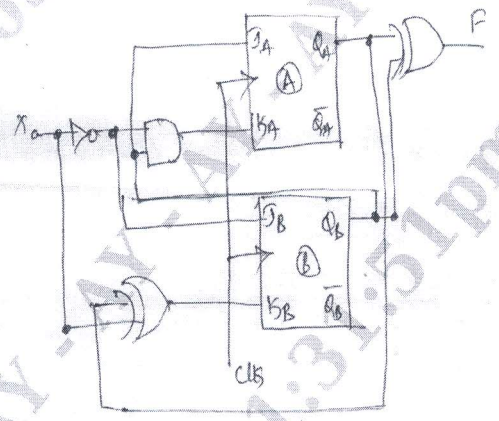
BEE306A

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Digital Logic Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Simplify using K-map, write the Boolean equation and realize using logic gates, $F(w,x,y,z) = \sum m(0,2,4,6,8) + \sum d(10,11,12,13,14,15)$	6	L2	CO1
	b.	Transform the following Boolean functions in to maxterm and minterm notation : (i) $F(w,x,y,z) = (\overline{w} + x)(y + z)$ (ii) $F(p,q,r) = \overline{pq} + pr$	6	L2	CO1
	c.	Simplify the following function using Quine Mc-Cluskey technique, $F(a,b,c,d) = \sum m(0,4,5,9) + \sum d(1,7,13)$	8	L3	CO1
		OR			
Q.2	a.	Simplify using K-map, $f(a,b,c,d) = \pi M(2,3,4,6,7,10,11,12)$	6	L2	CO1
	b.	Simplify using Quine Mc-Cluskey tabulation algorithm, $f(a,b,c,d) = \sum m(2,3,4,5,13,15) + \sum d(8,9,10,11)$	14	L3	CO1
		Module – 2			
Q.3	a.	Design 4 to 16 decoder using required number of 2 to 4 decoder IC's.	10	L4	CO2
	b.	Design and implement Two bit comparator using logic gates.	10	L4	CO2
		OR			
Q.4	a.	Implement $f(a,b,c,d) = \sum m(0,1,5,6,7,9,10,15)$ using, (i) 8 : 1 MUX with a, b, c as select lines (ii) 4 : 1 MUX with a, b as select lines	12	L3	CO2
	b.	Implement the following Boolean functions with suitable active high output decoders: (i) $f(w,x,y,z) = \sum m(3,7,9)$ (ii) $f(a,b,c) = \pi M(2,4,7)$	8	L3	CO2
		Module – 3			
Q.5	a.	Explain the operation of a gates SR latch with logic diagram and a truth table. Also high light the role of SR latch in switch debouncer circuit.	10	L2	CO3
	b.	Explain the operation of a positive edge triggered D flip flop with the help of a logic diagram, truth table and timing diagram.	10	L2	CO3
		OR			
Q.6	a.	Explain the operation of negative edge triggered JK flip flop with neat logic diagram, truth table and timing diagram.	10	L2	CO3

	b.	Obtain the characteristic equation for following flip flops : (i) SR flip flop (ii) JK flip flop	10	L3	CO3
		Module – 4			
Q.7	a.	Explain the following shift Register with logic and timing diagram : (i) SISO (ii) PIPO	10	L2	CO4
	b.	Write the design steps of Asynchronous counter. Also design mod-6 ripple counter using T-Flip Flops with negative edge.	10	L4	CO4
		OR			
Q.8	a.	Design and implement a mod-5 synchronous counter using JK flip-flops.	10	L4	CO4
	b.	Using positive edge triggering SR flip-flops design a counter which counts in the following sequence : 000, 111, 110, 101, 100, 011, 010, 001, 000…..	10	L4	CO4
		Module – 5			
Q.9	a.	Explain Mealy and Moore sequential circuit models.	8	L1	CO5
	b.	Construct the transition table, state table and state diagram for the Moore sequential circuit given below :  Fig. Q9 (b)	12	L4	CO5
		OR			
Q.10	a.	Design a cyclic modulo-8 synchronous counter using JK flip-flop that will count the number of occurences of an input, that is the number of times it is a 1. The input variable X must be coincident with the clock to be counted. The counter is to count in binary.	12	L4	CO6
	b.	Construct Moore and Mealy state diagram that will detect input sequence 10110 when input pattern is detected, Z is asserted high.	8	L4	CO5

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