CBCS SCHEME

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18CS33

Third Semester B.E. Degree Examination, June/July 2024
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the construction working and characteristics of Light Emitting Diode. **(06 Marks)**

b. With a neat circuit diagram and Mathematical analysis explain fixed bias circuit. **(07 Marks)**

c. Show how IC-555 timer can be used as Astable Multivibrator with Waveforms. **(07 Marks)**

OR

2 a. Discuss successive approximation register method of A to D converter with detailed conversion process. **(08 Marks)**

b. With neat diagram and waveform, explain working of inverting Schmitt trigger circuit. **(06 Marks)**

c. Explain Adjustable Voltage Regulator with diagram and suitable equations. **(06 Marks)**

Module-2

3 a. Simplify the following function using K-map and obtain simplified Boolean expressions:
$f_1(a, b, c, d) = \sum m(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13)$
$f_2(a, b, c, d) = \sum m(1, 3, 5, 7, 9) + \sum d(6, 12, 13)$. **(10 Marks)**

b. Simplify the following Boolean function by using Quine-Mcclusky (QM) method
$F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$. Find all the prime implicants. **(10 Marks)**

OR

4 a. Minimize the following function using MEV technique, use 'd' a MEV variable
$f(A, B, C, D) = \sum m(0, 1, 2, 7, 8, 9, 14, 15)$. **(08 Marks)**

b. With an example, explain Petrik's method. **(06 Marks)**

c. Solve the following clearly mention prime implicants and essential prime implicants
$f(a, b, c, d) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$. **(06 Marks)**

Module-3

5 a. What are Hazards in digital systems? Explain static 1 and static – 0 hazards. **(08 Marks)**

b. What is Multiplexer? Discuss 8 to 1 MUX with the help of logic diagram and equation. **(06 Marks)**

c. Discuss the importance of three state buffer with example. **(06 Marks)**

OR

6 a. Show how using a 3 to 8 decoder and multiinput or gates following Boolean expressions can be realized simultaneously
$F_1(A, B, C) = \sum m(0, 4, 6)$
$F_2(A, B, C) = \sum m(0, 5)$
$F_3(A, B, C) = \sum m(1, 2, 3, 7)$ **(06 Marks)**

b. Realize $f(a, b, c, d) = \sum m(1, 5, 6, 10, 13, 14)$ using AND-OR logic with number of levels, Gates and Gate inputs. **(06 Marks)**

c. Write a short note on PLA and PAL. **(08 Marks)**

Module-4

7 a. Discuss the operation of SR-Latch using NOR gates. Show how SR Latch can be used for switch debouncing. **(08 Marks)**

b. Explain Gated SR-latch using NAND gate. **(06 Marks)**

c. Differentiate between Latch and flip flop and explain the structure of VHDL program. **(06 Marks)**

OR

8 a. Explain the working operation of SR-flipflop and JK flip flop with truth table and waveforms. **(08 Marks)**

b. Draw the logic diagram of master slave JK flip flop using NAND gates and explain the working with suitable timing diagram. **(07 Marks)**

c. Discuss Toggle Flip Flop with truth table and characteristic equation. **(05 Marks)**

Module-5

9 a. Explain Parallel Adder with Accumulator with neat diagram and operation. **(08 Marks)**

b. What is Register? Explain how 4 bit register with data load clear and clock constructed using D flip flops. **(07 Marks)**

c. Discuss the operation of data transfer between Register. **(05 Marks)**

OR

10 a. Design the counter using D flip flop for the given sequence 0 – 3 – 2 – 6 – 4 – 7 – 0. **(08 Marks)**

b. Explain synchronous Binary Counter with logical diagram and transition table. **(06 Marks)**

c. Explain the working of 8 bit serial - in – serial - out shift register using SR flip flop. **(06 Marks)**

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