CBCS SCHEME

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21EE42

Fourth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define canonical minterm form and canonical maxterm form. **(05 Marks)**

b. Simplify the function using K-map,
$f(a,b,c,d) = \sum m(2,3,4,5,13,15) + \sum d(8,9,10,11)$. **(07 Marks)**

c. Simplify the given Boolean function using K-map and implement using logic gates :
$f(A,B,C,D,E) = \sum m(3,7,10,11,12,13,14,15,17,19,21,23,25,27,28,29,31) + \sum d(2,6,26,30)$.
(08 Marks)

OR

2 a. Define combinational logic, canonical SOP canonical POS and PI with examples. **(08 Marks)**

b. Obtain minimal SOP expression using Quine-McCluskey method and implement it using logic gates $f(a,b,c,d) = \sum m(0,1,4,5,9,11,13,15)$. **(12 Marks)**

Module-2

3 a. Implement Full Subtractor using a decoder and two NAND gates. Write its truth table. **(08 Marks)**

b. Design a two bit magnitude comparator and draw the logic diagram. **(12 Marks)**

OR

4 a. Implement the following using 8 : 1 MUX with a, b, c as select lines.
$f(a,b,c,d) = \sum m(0,1,5,6,7,9,10,15)$. **(08 Marks)**

b. Distinguish between a decoder and encoder. **(05 Marks)**

c. Explain briefly about Carry Look Ahead Adder. **(07 Marks)**

Module-3

5 a. Explain the working of Master Slave JK-Flip-Flops with functional table and neat timing diagrams. Show how race condition is overcome. **(12 Marks)**

b. Derive the characteristics equations for D, JK, T and SR FlipFlops. **(08 Marks)**

OR

6 a. Explain the working of SR Flip Flop along with truth table. Show the mechanism of switch debouncer using SR latch with neat waveforms. **(10 Marks)**

b. Discuss about positive and negative edge triggered D Flip Flop in brief. **(10 Marks)**

Module-4

7 a. Explain 4 modes of operation of shift register with suitable logic diagram and truth table. **(10 Marks)**

b. Design a MOD-5 synchronous binary counter using clocked JK Flip-Flops. **(10 Marks)**

OR

8 a. Briefly discuss about the working of 3-bit binary ripple counter with neat logic and timing diagrams. **(10 Marks)**

b. Design a 4-bit binary ripple up counter using positive edge triggered T-Flip Flop with a count enable line. Write the counting sequence and relevant timing diagram. **(10 Marks)**

Module-5

9 a. Design a sequential circuit using D-Flip Flop for the given state diagram. **(12 Marks)**

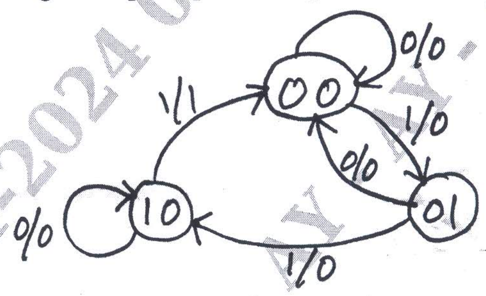

Fig. Q9 (a)

b. Explain the procedure of designing clocked synchronous sequential circuit with a suitable example. **(08 Marks)**

OR

10 a. Discuss briefly about Mealy and Moore models with neat block diagrams. **(08 Marks)**

b. Write brief notes on :
- (i) ROM
- (ii) RAM.
- (iii) EPROM
- (iv) Flash memory. **(12 Marks)**

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