CBCS SCHEME

USN | | | | | | | | | | |

15EC63

Sixth Semester B.E. Degree Examination, Dec.2023/Jan.2024
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Discuss the working of nMOS enhancement mode transistor operation with neat diagrams. **(06 Marks)**

b. Explain the CMOS inverter DC characteristics highlighting the regions of operation. **(10 Marks)**

OR

2 a. With neat diagrams discuss the nMOS fabrication process steps. **(09 Marks)**

b. Explain the following :

i) Channel length modulation ii) Noise Margin. **(07 Marks)**

Module-2

3 a. With a neat diagram, explain □ - rules for buried and butting contact and show the cross sectional view of same. (white any one structure burreid contact). **(08 Marks)**

b. Estimate the rise time and fall time of a CMOS inverter and summarise the result. **(08 Marks)**

OR

4 a. Define Sheet resistance, with equation. **(02 Marks)**

b. Calculate the area capacitance of the layer below [Refer Fig. Q4(b)] :

Fig. Q4(b)

i) If the layer is metal – 1 and relative capacitance value is 0.075

ii) If the layer is polysilicon and relative capacitance value is $0.1 \square C_g$. if the layer is polysilicon and relative capacitance value is $0.1 \square C_g$. **(06 Marks)**

c. Write the schematic and stick diagram for Boolean expression $y = \overline{(a + bc)}$. (Implement using CMOS logic). **(08 Marks)**

Module-3

5 a. Explain the constant field, constant voltage scaling models with a diagram and scaling effect table. **(06 Marks)**

b. Discuss the problems associated in VLSI design. How do you reduce them? **(05 Marks)**

c. Discuss the different bus architectures. **(05 Marks)**

OR

6 a. Discuss the design of a 4-bit adder. **(07 Marks)**

b. With relevant diagram, discuss Manchester carry chain operation. **(05 Marks)**

c. Explain the carry select adder with a diagram. **(04 Marks)**

Module-4

7 a. Discuss the architectural issues to be followed in the design of VLSI sub system. **(05 Marks)**
b. Explain in detail the general structure of an FPGA fabric. **(06 Marks)**
c. Explain switch logic implementation of CMOS 5 way selector, with neat circuit diagram. **(05 Marks)**

OR

8 a. Explain the structured design approach for implementation of a parity generator. **(08 Marks)**
b. Explain Dynamic CMOS logic with example. **(08 Marks)**

Module-5

9 a. Write the system timing considerations. **(08 Marks)**
b. Explain Logic verification principle. **(08 Marks)**

OR

10 a. Explain Three transistor dynamic RAM, with neat circuit and stick diagram. **(06 Marks)**
b. What are Design manufacturability. **(10 Marks)**

* * * * *