# GBGS SCHEME

Sixth Semester B.E. Degree Examination, Dec.2023/Jan.2024  Digital System Design Using Verilog  Time: 3 hrs.  Note: Answer any FIVE full questions, choosing ONE full question from each module.  Module-1  1 a. Discuss the design methodology in detail along with flowchart.  b. Develop verilog model for a 7-segment decoder include an additional input blank that overrides the BCD input and causes all the segments not to be lit.  (08 Marks)  C. What values are represented by the 8 bit 2-s complement numbers 00110101 and 101101017  (04 Marks)  OR  2 a. Explain the effects of capacitance loading and propagation delay on signal transitions between logic levels.  b. Construct a data path to perform complex multiplication of two complex number whose real and imaginary parts are represented as signed fixed point numbers with 4-prebinary and 12 post binary points. Real and imaginary parts of the product are represented with 8 prebinary points and 24 post binary points. Area is the main constraint. Also write verilog model of complex multiplier data path.  Module-2  3 a. Design 64K × 8 bit composite memory using for 16K × 8 bit components. (06 Marks)  b. Differentiate between flow through and pipe lined SSRAM with neat timing diagram.  (10 Marks)  OR  4 a. Develop a veriolog model of a dual port 4K × 16bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. (08 Marks)  Determine whether there is an error in the ECC word 111011011101 and if SO correct it.  (06 Marks)  C. Explain dynamic RAM operation.  Module-3  5 a. Define the following in IC fabrication  i) Ion implantation  ii) Etching  iii) Photo resists  iv) Defect and yield.  b. Write and explain internal organization of CPLD. (08 Marks)	USN			18EC644	
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c. Distinguish between surface mount IC packages from insertion type packages. (04 Marks)			Distinguish between surface mount IC packages from insertion type packages.		

#### OR

- 6 a. Explain about internal organization of FPGA with neat diagram. (10 Marks)

  b. Explain signal integrity and differential signaling. How does differential signaling improve
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## Module-4

- 7 a. Explain any four Analog input sensors. (08 Marks)
  - b. Explain Flash ADC and SAR ADC with diagrams. (12 Marks)

### OR

- 8 a. Design an input controller that has 8 bit binary coded input from a sensor. The value can be read from a 8 bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system. Also write verilog model. (08 Marks)
  - b. Explain the concept of multiplexed Buses. (04 Marks)
  - c. Discuss the serial interface standard for I/O devices. (08 Marks)

## Module-5

- 9 a. Discuss Hardware, Software Co-design methodology in detail with flow chart. (08 Marks)
  - b. Explain area and power optimization in detail. (06 Marks)
  - c. Explain Functional design and Functional verification. (06 Marks)

#### OR

- 10 a. Explain scan design and boundary scan in detail. (08 Marks)
  - b. With neat diagram, explain 4-bit LFSR and CPSR for generating Pseudo-random test vectors.

    (08 Marks)
  - c. Explain Fault model. (04 Marks)

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