CBCS SCHEME

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17EC45

Fourth Semester B.E. Degree Examination, Dec.2023/Jan.2024
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With the help of basic op-amp circuit, investigate the circuit operation for assuming that $V_{CC} = +10V$, $V_{EE} = -10V$, $R_E = 4.7K\Omega$, $R_C = 6.8K\Omega$ and all transistors having $V_{BE} = 0.7V$. **(08 Marks)**

b. Using a 741 op-amp, design a non-inverting amplifier to have a voltage gain of 66. The input signal amplitude is to be 15mV. **(06 Marks)**

c. Derive the output voltage equation of a two input non-inverting summer. **(06 Marks)**

OR

2 a. Define the following op-amp parameters and mention its typical value for 741 op-amp.
i) CMRR ii) PSVR iii) Slew rate iv) Input offset current. **(08 Marks)**

b. The difference of two input signal is to be amplified by a factor of 37. Each input has an amplitude of 50mV. Using an LF353 op-amp. Design a suitable and calculate the differential and common mode input resistances. **(06 Marks)**

c. Explain the biasing of a op-amp using potential divider bias with both polarity supply and also mention equation for calculating R_1 and R_2. **(06 Marks)**

Module-2

3 a. Explain the operation of a high Z_{in} capacitor coupled voltage follower and show that $Z_{in} = R_1(1 + M)$. **(08 Marks)**

b. Design a capacitor coupled inverting amplifier is to have a voltage gain of 50 and produces an output of 3V. The lower cut off frequency is 300Hz and load resistance is 6KΩ. Use 741 op-amp. **(06 Marks)**

c. Explain the operation of a current amplifier and mention its disadvantage. **(06 Marks)**

OR

4 a. Explain the working principles of capacitor coupled non-inverting amplifier and write the mathematical equations for solving C_1 and C_2. **(08 Marks)**

b. Design inverting amplifier is to be capacitor coupled and to have a signal frequency range of 10Hz to 1KHz. If the load resistance is 250Ω. Use 741 op-amp with $A_V = 50$ and $V_0 = 3V$. **(06 Marks)**

c. Explain the working of low resistance voltage source. **(06 Marks)**

Module-3

5 a. Explain the working of sample and Hold circuit using op-amp. **(08 Marks)**

b. Using a 741 op-amp with a supply of ± 12V, design a phase shift oscillator to have an output frequency of 3.5KHz. **(06 Marks)**

c. Discuss the working principles of analog multiplier and mention its applications. **(06 Marks)**

OR

6 a. Design a inverting Schmitt trigger circuit using 741 op-amp with a ± 18V supply to have UTP = 1.5V and LTP = –3V. Assume silicon diode with $V_F = 0.7V$ and $R_1 = 27K\Omega$. **(08 Marks)**

b. Explain the working of Wein bridge oscillator using op-amp. **(06 Marks)**

c. Prove that $V_0 = \frac{-KT}{q} \ell n\left(\frac{V_{in}}{V_{ref}}\right)$ of a log amplifier. **(06 Marks)**

Module-4

7 a. Explain the working of first order active low pass filter and also write the design equations. **(08 Marks)**

b. Design a second order active high pass filter to have a cutoff frequency of 12KHz. Use a 715 op-amp with $I_{B(max)} = 1.5\mu A$. **(06 Marks)**

c. Draw the functional block diagram of 723 regulator and mention the function of each element. **(06 Marks)**

OR

8 a. What are the Four important characteristics of 3 – terminal IC regulator and explain it. **(08 Marks)**

b. Design an adjustable regulator from the 7810 regulator to get on output of 15V. Assume $I_{R1} = 50mA$ and $I_Q = 4.2mA$. **(06 Marks)**

c. Explain the operation of Narrow Bandpass filter. **(06 Marks)**

Module-5

9 a. Draw the block diagram of PLL and mention functions of each block. **(08 Marks)**

b. What output voltage would be produced by a DAC whose output range is 0 to 10V and whose input binary are : i) 10 ii) 0110 iii) 1011100. Assume $R_F = R = 1k\Omega$. **(06 Marks)**

c. Design an Astable multivibrator using 555 timer to provides output frequency of 1KHz and duty cycle of 60%. Assume $C = 0.1\mu F$. **(06 Marks)**

OR

10 a. Explain the operation of a successive approximation ADC. **(08 Marks)**

b. Define the following parameters of PLL :
i) Lock in Range
ii) Capture Range
iii)Pull–in time. **(06 Marks)**

c. Designs a monostable multivibrator using 555 Timer with pulse width of 0.25m sec. Derive the equation required for designing a multivibrator. Assume $C = 0.1\mu F$. **(06 Marks)**

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