MAKE-UP EXAM

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BETCK205J/ BETCKJ205

Second Semester B.E./B.Tech. Degree Examination, Nov./Dec.2023
Introduction to Embedded System

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define embedded system? Give the classification of embedded systems based on generation and complexity and performance.	8	L2	CO1
	b.	Explain the role of watchdog timer in embedded system.	6	L2	CO1
	c.	Differentiate between microprocessor and microcontroller.	6	L2	CO1
		OR			
Q.2	a.	Describe with neat diagram the concept of load store architecture and instruction pipelining.	8	L2	CO1
	b.	What are the different types of memories used in Embedded system? Illustrate the role of each in embedded system.	6	L3	CO1
	c.	With neat diagram, explain the I2C (Inter Integrated Circuit) Bus interface.	6	L2	CO1
		Module – 2			
Q.3	a.	Explain any 5 characteristics of embedded systems.	10	L2	CO1
	b.	With neat graph, explain the product life cycle in embedded system product development.	6	L2	CO1
	c.	Explain the different Electronic Control Units (ECU's) used in automotive system.	4	L2	CO1
		OR			
Q.4	a.	Describe different communication buses used in automotive embedded applications.	10	L2	CO1
	b.	With functional block diagram, explain the operation of washing machine.	6	L3	CO5
	c.	Describe time to prototype and market of non-operational quality attribute of embedded system.	4	L2	CO1
		Module – 3			
Q.5	a.	What is hardware software co-design in embedded system? Explain the fundamental issues in hardware software co-design.	10	L2	CO3
	b.	With block diagram and Truth table, explain the operation of 3-8 decoder.	6	L2	CO3
	c.	Design an automatic tea/coffee vending machine using FSM model. Requirements : The tea/coffee vending machine is initiated by the user inserting a 5 rupee coin. After inserting coin, the user can either select "Coffee" or "Tea" or press "Cancel" to cancel the order and take back the coin.	4	L3	CO5
		OR			

Q.6	a.	With neat diagram, explain the synchronous 3 bit binary counter using Flip-flops.	8	L2	CO5
	b.	Construct 2-input half adder using basic gates and draw the logic diagrams and truth table.	6	L3	CO5
	c.	Explain with diagram and example the Data Flow Graph (DFG) model in embedded system.	6	L2	CO4
		Module – 4			
Q.7	a.	Explain with example the super loop based approach in embedded Firmware design.	8	L2	CO4
	b.	Explain the format of HEX records in an intel/HEX file.	6	L2	CO4
	c.	Describe the following : (i) Library file creation and usage. (ii) Linker and locator. (iii) Object to hex file converter	6	L2	CO4
		OR			
Q.8	a.	Explain the various details held by a list file generated during the process of cross-compiling an embedded "C" project.	8	L2	CO4
	b.	Describe with neat diagram, the Assembly language to machine language conversion process.	6	L2	CO4
	c.	What are the different techniques available for embedded firmware debugging? Explain the incremental EEPROM Burning technique.	6	L2	CO2
		Module – 5			
Q.9	a.	What is Task Control Block (TCB)? Explain the structure of TCB in Task management of the Real time Kernel.	8	L2	CO2
	b.	Describe with diagrams the monolithic kernel and microkernel.	6	L2	CO2
	c.	Differentiate between Hand and Soft Real time system? Give examples for each.	6	L2	CO2
		OR			
Q.10	a.	Explain with diagram Round robin preemptive scheduling and calculate the waiting time and Turn Around Time (TAT) for each process and the average waiting time and turn around time of three processes with process IDs. P_1, P_2 and P_3 with estimated completion time of 6, 4, 2 milliseconds respectively, enters the ready queue together in the order P_1, P_2 and P_3. The time slice is : 2 ms.	8	L3	CO5
	b.	Differentiate between thread and process in context with RTOS.	6	L2	CO2
	c.	With neat diagram, explain process states and state transitions in RTOS.	6	L2	CO2

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