

CBCS SCHEME

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17MT35

Third Semester B.E. Degree Examination, June/July 2023 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Design a second order lowpass Butterworth filter at a higher cutoff frequency of 1KHz and draw the frequency response. (10 Marks)
- b. Design a highpass filter at a cutoff frequency of 1KHz with a passband gain of 2 and plot the frequency response. (10 Marks)

OR

- 2 a. Design a wide bandpass filter with $f_c = 200\text{Hz}$ and $f_H = 1\text{ KHz}$ and passband gain = 4 and draw the frequency response. (10 Marks)
- b. With neat diagram, explain all pass filter and derive the expression for gain and phase angle. (10 Marks)

Module-2

- 3 a. Derive the equations that explain the two criteria required to be fulfilled for oscillator. (10 Marks)
- b. With a neat circuit diagram, explain phase shift RC oscillator. (05 Marks)
- c. Design the phase shift oscillator for frequency of oscillation $f_0 = 300\text{Hz}$. (05 Marks)

OR

- 4 a. With the help of I/P and O/P waveforms explain the working of zero crossing detector. (10 Marks)
- b. For Schmitt trigger circuit, explain the following : (10 Marks)
 - i) Upper Trigger Point (UTP)
 - ii) Lower Trigger Point (LTP)
 - iii) Plot of Hysteresis Voltage.

Module-3

- 5 a. With neat diagrams, explain the pin diagram and architecture of 555 Timer. (10 Marks)
- b. Explain the operation of 555 Timer as a monostable multi-vibration with necessary diagrams. (10 Marks)

OR

- 6 a. Explain the operation of 555 Timer as an Astable multivibrator with necessary diagram. (10 Marks)
- b. With neat circuit diagrams, explain the applications of astable multivibrator. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. Explain the full adder circuit with the following : (10 Marks)
i) Truth table ii) Logic Diagram.
b. Explain the working of 4×1 MUX with operation table, select lines and logic diagram. (10 Marks)

OR

- 8 a. Map the following function on K' map $F(A, B, C, D) = \Sigma 1, 5, 6, 9, 14, 15$. (06 Marks)
b. Implement the following function using 4×1 MUX. $F(A, B, C) = \Sigma 1, 3, 5, 7$. (10 Marks)
c. Draw the K' map for three variables. (04 Marks)

Module-5

- 9 a. With neat circuit analyze the operation of clocked JK Flip Flop. Also derive the characteristic equation from truth table. (10 Marks)
b. Design a synchronous 3 bit binary upcounter using the excitation table. (10 Marks)

OR

- 10 a. Design BCD Ripple counter. (10 Marks)
b. With a neat circuit analyze the operation of clocked SR flip flop using NOR latch. Also derive the characteristic equation from truth table. (10 Marks)
