CBCS SCHEME

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15MT35

Third Semester B.E. Degree Examination, June/July 2023
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Sketch and explain the VI characteristics of diode with current equation and comparison with ideal, Germanium and Silicon diode. **(08 Marks)**

b. Calculate the magnitude of the diode current (I_A) for the following values of the diode junction voltage (V_{AK}).

i) $V_{AK} = -0.5V$
ii) $V_{AK} = -0.10V$
iii) $V_{AK} = 0.25V$
iv) $V_{AK} = 0.35V$
v) $V_{AK} = 0.6V$
vi) $V_{AK} = 0.75V$
vii) $V_{AK} = IV$.

The reverse saturation current, I_R of p-n junction silicon diode is 100nA. Assume the thermal voltage $V_T = 27mV$ at $T = 300K$. **(08 Marks)**

OR

2 a. Describe clipping and clamping circuits with circuit diagram and waveforms with applications. **(08 Marks)**

b. A full wave rectifier produces an rms voltages of 12V from a 50Hz line source and feeds a resistive load of 1.5Ω. If the filter uses a capacitance C = 470μF. Find the resulting

i) Output ripple factor
ii) dc output voltage V_{LDC}
iii) Voltage regulation
iv) The ripple output voltage V_r. **(08 Marks)**

Module-2

3 a. Evaluate the expression for gain of a first order Butterworth low pass filter. Plot the frequency response. Also mention the design steps. **(10 Marks)**

b. Evaluate the low cutoff frequency for the second order high pass Butterworth filter. Given $C_2 = C_3 = 0.0047\mu F$, $R_2 = R_3 = 33\ K\Omega$ and also draw the circuit diagram. **(06 Marks)**

OR

4 a. With a neat circuit analyze the working of RC phase shift oscillator. Using OPAMP design a RC phase shift oscillator to have $F_0 = 2$ kHz. **(10 Marks)**

b. Design a first order low pass filter of cut off frequency 1 kHz with a pass band gain of 2 and using frequency sealing technique convert 1 kHz cut off frequency to 1.6 kHz. **(06 Marks)**

Module-3

5 a. With a neat circuit and relevant waveforms analyze inverting comparator as Schmitt trigger. And also design a Schmitt trigger circuit with $V_{ut} = +3V$ and $V_{lt} = -3V$. With supply voltage of ±15V. If supply voltage is 10V(P – P). Find hysteresis voltage. **(10 Marks)**

b. Design a divide by 2 network using a monostable multivibrator for input trigger signal of 2 kHz and c = 0.1 μF. **(06 Marks)**

OR

6 a. Discuss the working of a Astable multivibrator circuit with neat block and waveforms. **(10 Marks)**

b. With a neat circuit and waveforms analyze the working of a non-inverting comparator circuit. **(06 Marks)**

Module-4

7 a. i) By using NOR gate, implement the following gates.
1) NOT 2) OR 3) AND 4) EX-OR and EX-NOR. **(05 Marks)**

ii) Implement EX-OR and EX-NOR using NAND gates. **(03 Marks)**

b. i) Draw C-MOS NOR gate and C-MOS NAND gate for different input combinations A. **(05 Marks)**

ii) Compare TTL, C-MOS and ECL logic families. **(03 Marks)**

OR

8 a. Explain operation of RS-latch using NAND gate and NOR gate with circuit diagram, and different input combinations (truth – table) **(08 Marks)**

b. Explain the operation of J-K flip flop with diagram and different input combination using truth table and its characteristics equation. **(08 Marks)**

Module-5

9 a. Implement the following Boolean function using the depth understanding of MUX.
$f(x, y, z) = \varepsilon m(1, 2, 4, 6, 7)$ **(06 Marks)**

b. Analyze the working of successive approximation type ADC with neat sketch. Also obtain the 4 bit binary representation of analog signal 10-7 V using successive approximation technique. Full scale voltage = ±16V. **(10 Marks)**

OR

10 a. Discuss the operation of weighted resistor 4 bit DAC with necessary circuit and equations. **(06 Marks)**

b. Analyze the working of 2 × 4 decoder circuit and also design a 3 × 8 decoder using 2 × 4 decoder. **(10 Marks)**

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