CBCS SCHEME

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21MT32

Third Semester B.E. Degree Examination, June/July 2023
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the equation for the voltage gain of a first order High Pass Active Filter and briefly discuss the circuit design procedure. **(12 Marks)**

b. Design a Low Pass filter at a cutoff frequency of 1 kHz with a Passband gain of 2. Choose C = 0.01 μF. **(08 Marks)**

OR

2 a. Derive the expression for the phase shift produced by an All Pass Filter. **(12 Marks)**

b. With neat circuit, frequency response diagram and with necessary equations, explain the operation of wide band pass filter. **(08 Marks)**

Module-2

3 a. With neat circuit diagram, explain the operation of wein bridge oscillator. **(12 Marks)**

b. Using a 741 op-amp with a supply of ±12V, design a RC phase shift oscillator to have an output frequency of 3.5 kHz. **(08 Marks)**

OR

4 a. Explain the operation of Schmitt trigger with neat circuit diagram, waveforms and hysteresis curve. **(12 Marks)**

b. Explain the operation of Inverting Comparator with circuit diagram and waveforms. **(08 Marks)**

Module-3

5 a. With neat diagram, explain the pin diagram and internal architecture of 555 timer. **(12 Marks)**

b. With a neat sketch, explain how to construct a square wave generator from Astable Multivibrator. **(08 Marks)**

OR

6 a. Explain the operation of 555 time as Astable Multivibrator. **(12 Marks)**

b. How is an Monostable Multivibrator using 555 timer connected into a pulse width modulator. **(08 Marks)**

Module-4

7 a. Simplify the following Boolean equation using K-Maps.

(i) $f(w, x, y, z) = \sum m(1, 3, 6, 9, 11, 14, 15)$ **(05 Marks)**

(ii) $f(a, b, c, d) = \Pi M(0, 2, 4, 10, 11, 14, 15)$ **(05 Marks)**

b. Implement a Full Adder circuit using two Half Adders. **(10 Marks)**

OR

8 a. Implement the function using 4:1 MUX with a, b as select lines:
$f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$ **(10 Marks)**

b. Explain the operation of 3 to 8 line decoder with truth table and logic diagram. **(10 Marks)**

Module-5

9 a. Explain the operation of clocked RS-flip flop using NAND gates with timing diagram and truth table. **(10 Marks)**

b. Explain the operation of clocked D-flip flop using NAND gates with timing diagram and truth table. **(10 Marks)**

OR

10 a. Explain the operation of synchronous 3-bit binary Up-counter. **(10 Marks)**

b. Explain the operation of
(i) Decade counter using IC 7490 **(05 Marks)**
(ii) Ring counter using IC 7495 **(05 Marks)**

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