CBCS SCHEME

USN | | | | | | | | | | |

18EC644

Sixth Semester B.E. Degree Examination, June/July 2023
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What are the effects of capacitive loading and propagation delay on signal transitions between logic level? **(10 Marks)**

b. Develop a verilog model for a 7-segment decoder that includes an additional input, "BLANK" that overrides the BCD input and causes all segments not to lit. **(10 Marks)**

OR

2 a. Discuss about fixed point numbers and fixed-point representation in verilog. **(10 Marks)**

b. Explain the synchronous timing methodologies. **(10 Marks)**

Module-2

3 a. Design a 16K × 48-bit memory using 16K × 16-bit memory component. **(08 Marks)**

b. Explain flow through and pipelined SSRAM with the help of timing diagram. **(12 Marks)**

OR

4 a. Develop a verilog model of a dual-port 4K × 16 bit flow through SSRAM. One port allows data to be written and read. While the other port allows data to be read. **(10 Marks)**

b. Determine whether there is an error in the ECC word "000111000100", and if so, correct it. **(05 Marks)**

c. Discuss about multiport memories. **(05 Marks)**

Module-3

5 a. Explain the internal organization of a CPLD, with neat diagram. **(10 Marks)**

b. Explain different types of packaging and circuit boards. **(10 Marks)**

OR

6 a. Define signal integrity. Discuss ground bounce issue in signal integrity and technique used to reduce ground bounce effect. **(10 Marks)**

b. Discuss the internal architecture of FPGA. **(10 Marks)**

Module-4

7 a. With a neat figure, explain flash ADC and SAR ADC. **(10 Marks)**

b. Discuss about multiplexed buses, with neat figure. **(10 Marks)**

OR

8 a. Explain the following serial interface standards.
i) RS – 232 ii) I^2C. **(10 Marks)**

b. Explain the following I/O synchronization techniques:
i) Polling ii) Interrupts. **(10 Marks)**

Module-5

9	a.	Explain the design flow of hardware/software codesign.	(10 Marks)
	b.	Explain floor plan, placement and routing of ASIC physical design.	(10 Marks)

OR

10	a.	Explain the concepts of scan design and boundary scan.	(10 Marks)
	b.	Explain Built-In Self Test (BIST) techniques.	(10 Marks)

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