CBCS SCHEME

USN | | | | | | | | | | |

15EC63

Sixth Semester B.E. Degree Examination, June/July 2023
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive the CMOS inverter DC characteristics graphically from p device and n device characteristics and show all operating regions. **(08 Marks)**

b. Explain the working of nMOS enhancement mode transistor with suitable diagrams. **(08 Marks)**

OR

2 a. Derive expression for drain current in linear and saturation region for nMOS transistor. **(08 Marks)**

b. With neat sketches explain the CMOs P-well process steps to fabricate a CMOS inverter. **(08 Marks)**

Module-2

3 a. Discuss the CMOS design style with a diagram. **(05 Marks)**

b. Draw the stick diagram for the following using CMOS logic :

i) $Y = \overline{A + B + C}$ ii) 2 i/p NAND gate. **(05 Marks)**

c. Discuss the different contact cuts with an example to each. **(06 Marks)**

OR

4 a. With a diagram derive an expression for sheet resistance and mention the R_s values of metal, p and n transistor channels for 5 μm technology. **(05 Marks)**

b. Derive an equation for rise time and fall time with respect to CMOS inverter. **(08 Marks)**

c. Draw the circuit and stick diagram for 2 i/p NOR gate using CMOS logic. **(03 Marks)**

Module-3

5 a. Design 4bit, 4 × 4 barrel shifter. Write the nMOS implementation and strategy for the same. **(08 Marks)**

b. Explain Carry select adder with neat block diagram. **(08 Marks)**

OR

6 a. Define Regularity. **(02 Marks)**

b. Derive the scaling factor for the device parameter :

i) Parasitic capacitance ii) Channel resistance iii) Gate delay. **(06 Marks)**

c. Implement the ALU functions like EX – OR, EX – NOR AND and OR operations with an adder. Write the block diagram of 4 – bit ALU using adder element. **(08 Marks)**

Module-4

7 a. Discuss the programmable logic array with its structure and floor plan. **(05 Marks)**

b. Discuss the architectural issues related to VLSI sub system design. **(06 Marks)**

c. Discuss the design of Data selectors. **(05 Marks)**

OR

8 a. Explain the architecture of field programmable gate array. **(10 Marks)**
b. Discuss the FPGA abstractions with a diagram. **(06 Marks)**

Module-5

9 a. Explain 3 transistor dynamic RAM cell with schematic diagram. **(06 Marks)**
b. Explain any two fault models in combinational circuits. **(06 Marks)**
c. Write a note on automatic test pattern generation. **(04 Marks)**

OR

10 a. Write short notes on :
i) Observability and Controllability.
ii) Built In Self Test (BIST). **(08 Marks)**
b. Explain nMOS pseudo static RAM cell with schematic diagram. **(08 Marks)**

* * * * *