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10EC63

Sixth Semester B.E. Degree Examination, June/July 2023
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: 1. Note: ***Answer any FIVE full questions, selecting atleast THREE questions from Part-A and any TWO questions from Part-B.***

2. State all assumptions, including missing data.

PART – A

1 a. Explain channel length modulation and derive the equation for finite output resistance of a MOSFET in saturation. **(08 Marks)**

b. Explain the role of substrate in V_t variation. **(04 Marks)**

c. Design the circuit shown in Fig Q1(c), to establish a dc drain current I_D = 0.5mA. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having same $K_n' W/L$ but V_t = 1.5V. Neglect the channel length modulation effects.

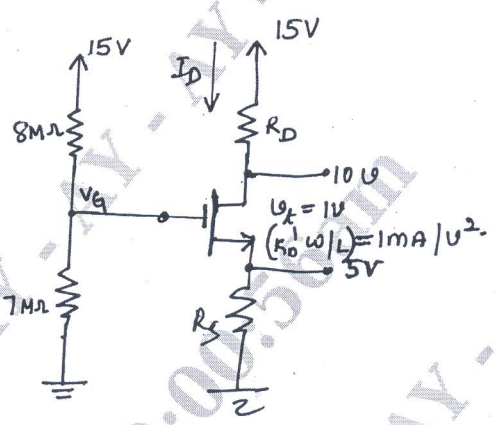

Fig Q1(c) **(08 Marks)**

2 a. Obtain an expression for R_{in}, A_v, A_{Vo}, G_V and R_{out} for CG amplifier circuit using MOSFET. **(10 Marks)**

b. Explain the development of the T-equivalent circuit model for MOSFET. **(05 Marks)**

c. Mention any 5 comparison of important characteristics of MOSFET and BJT. **(05 Marks)**

3 a. Explain the various short channel effects due to scaling. **(10 Marks)**

b. For the high frequency equivalent circuit of a common source amplifier shown in Fig Q3(b), having R_{sig} = 100KΩ, R_{in} = 420KΩ, $C_{gs} = C_{gd}$ = 1 Pt, g_m = 4mA/u, and R_L' = 3.33 KΩ. Find the midband voltage gain $\left(\frac{u_0}{u_{sig}}\right)$ and upper 3-db frequency f_H.

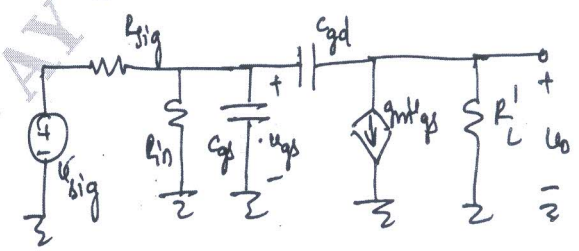

Fig Q3(b) **(10 Marks)**

4 a. Consider a common – gate amplifier specified as follows : $W/L = 7.2\mu m/0.36\mu m$, $\mu_n C_{ox} = 387\mu A/V^2$, $r_0 = 18K\Omega$, $I_D = 100\mu A$, $g_m = 1.25mA/V$, $\lambda = 0.2$, $R_s = 10K\Omega$, $R_L = 100K\Omega$, $C_{gs} = 2fF$, $C_{gd} = 5fF$ and $C_L = 0$. Find : $A_{v0} = R_{in}$, R_{out}, G_V, G_{is}, G_i and f_H. **(10 Marks)**

b. What is cascade amplifier and explain the folded cascade circuit. **(05 Marks)**

c. Explain Wilson MOS current mirror circuit. **(05 Marks)**

5 a. Draw and explain the circuit diagram of a active load MOS differential pair and derive an expression for G_m. **(12 Marks)**

b. Explain a two stage CMOS opamp with neat circuit diagram. **(08 Marks)**

PART – B

6 a. Explain the properties of negative feedback with required expressions. **(10 Marks)**

b. Explain the effect of negative feedback on input resistance, output Resistance and gain of an ideal series shunt feedback amplifier. **(10 Marks)**

7 a. Explain instrumentation amplifier with neat circuit diagram and list the advantages and disadvantages of it. **(10 Marks)**

b. Derive an expression for an input resistance of the investing amplifier, where A is the finite open loop gains. **(05 Marks)**

c. For the logarithm amplifier shown in Fig Q7(c). Prove that output voltage V_0 is the logarithm of the input signal.

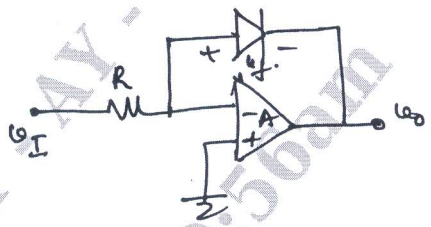

Fig Q7(c) **(05 Marks)**

8 a. Explain the parameters used to characterize, the operation and performance of a logic circuit family. **(08 Marks)**

b. Draw a CMOS logic circuit that realizes the function $F = \overline{(A+B)(C+D)}$ **(04 Marks)**

c. Provide transistor (W/L) ratios for the logic circuit shown in Fig Q8(c). Assume that for the basic inverter n = 1.5 and P = 5 and the channel length is 0.25μm.

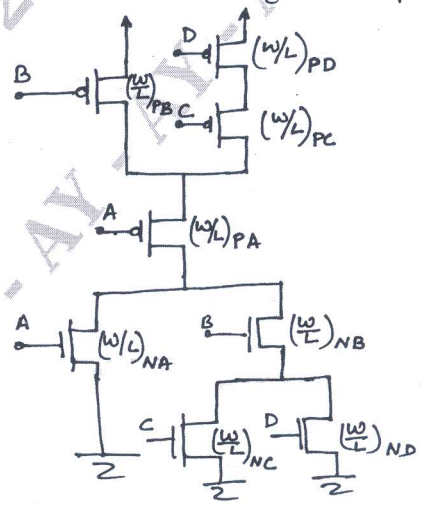

Fig Q8(c) **(08 Marks)**