CBCS SCHEME

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17EC33

Third Semester B.E. Degree Examination, June/July 2023
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Derive an expression for A_V, Z_i, and Z_0 for CE –fixed bias using r_e equivalent model. **(10 Marks)**

b. What is an emitter follower? Discuss about emitter follower circuit and find Zi, Z_0 and A_v using r_e – model. **(10 Marks)**

OR

2 a. Define h-parameters and derive h-parameters model of CE – BJT. **(10 Marks)**

b. For an emitter – bias circuit (capacitor is unbypassed), determine r_e, Z_i, Z_0 and A_V. Given $R_B = 470K\Omega$, $R_C = 2.2K\Omega$, $V_{CC} = 20V$, $R_E = 0.56K\Omega$, $C_E = 10\mu F$, $\beta = 120$, $r_0 = 40K\Omega$, $C_C = 10\mu F$. **(10 Marks)**

Module-2

3 a. For the self-bias configuration shown has an operating point $V_{GSQ} = -2.6V$ and $I_{DQ} = 2.6mA$ with $I_{DSS} = 8mA$ and $V_p = -6V$. Assume $Y_{OS} = 20\mu S$. (Refer Fig.Q3(a)).
Find : i) g_m ii) r_d iii) Z_i iv) Z_0 v) A_V.

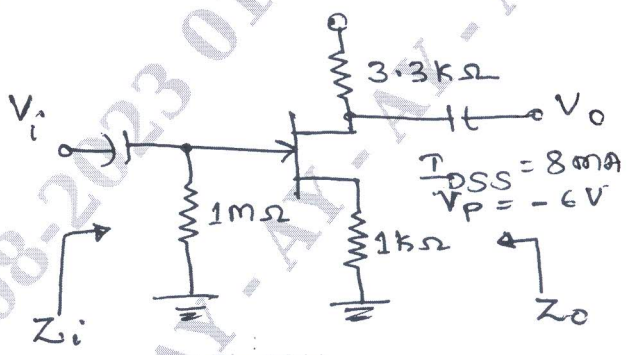

Fig.Q3(a) **(10 Marks)**

b. Derive an expression for Z_i, Z_0 and A_V for JFET source follower circuit using small signal model. **(10 Marks)**

OR

4 a. Explain the small-signal model of the FET. **(10 Marks)**

b. Write the ac equivalent circuit for voltage – divider JET configuration. Determine Z_i, Z_0 and A_V. **(10 Marks)**

Module-3

5 a. Determine :

i) The common logarithm of the number 2.2×10^3

ii) The power gain is decibles for $P_0 = 100$m walts, $P_i = 5$m watts

iii) Find voltage gain in dB for o/p voltage 100V and $R_0 = 20\Omega$. **(08 Marks)**

b. Prove that miller effect of input capacitance. $C_{mi} = (1 - A_V) C_f$ and output capacitance

$$C_{m_0} = \left(1 - \frac{1}{A_v}\right) C_f .$$ **(12 Marks)**

OR

6 a. Derive an expression for high – frequency response of FET amplifier. **(12 Marks)**

b. Discuss the effect of various capacitors on multistage frequency response. **(08 Marks)**

Module-4

7 a. Discuss about the different types of feedback connections indicating input and output signal. **(12 Marks)**

b. With a neat circuit diagram, explain the working principle of FET RC–phase–shift oscillator. **(08 Marks)**

OR

8 a. What are the effects of negative feedback in an amplifier? Show how bandwidth of an amplifier increases with negative feedback. **(10 Marks)**

b. A crystal has the following parameter $L = 0.334$H, $C_m = 1$pF, $C = 0.065$pF and $R = 5.5$KΩ. Calculate the series resonant and parallel resonant frequency and Q of the crystal. **(10 Marks)**

Module-5

9 a. With a neat circuit diagram explain the operation of a transformer coupled class A power amplifier. **(10 Marks)**

b. For the following distortion values, calculate :

i) THD

ii) Fundamental power component

iii) P_t.

Given : $D_2 = 0.2$, $D_3 = 0.02$, $D_4 = 0.06$, $I_L = 3.3$A and $R_C = 4\Omega$. **(10 Marks)**

OR

10 a. With a neat circuit diagram, explain the working principle of complementary symmetry push – pull amplifier. **(10 Marks)**

b. With a neat circuit diagram, explain the working principle of fold back current limiting circuit. **(10 Marks)**

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