



# CBCS SCHEME

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17EC34

Third Semester B.E. Degree Examination, June/July 2023

## Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. Place the given equations into proper canonical form:
- (i)  $P = f(a, b, c) = \overline{a}b + \overline{a}c + abc$
- (ii)  $S = f(x, y, z) = \overline{x}y + xz + \overline{y}z$  (08 Marks)
- b. For a given truth-table, write the SOP and POS expressions and design logic circuit for both. (Refer Truth table of Fig.Q1(b)) (08 Marks)

Input			Output
a	b	c	y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Fig.Q1(b) : Truth Table

(04 Marks)

OR

- 2 a. Simplify  $y = f(a, b, c, d) = \Sigma(1, 3, 5, 6, 8, 10, 12) + d(0, 4, 7, 14)$  using K-map method and draw the logic circuit for obtained expression using NAND gates. (10 Marks)
- b. Simplify  $y = f(a, b, c, d) = \Sigma m(0, 1, 2, 4, 6, 8, 9, 12, 14)$  using QM method. Verify using K-map technique. (10 Marks)

### Module-2

- 3 a. Using a 2 to 4 decoder IC-74LS139, realize a Boolean function  $S = f(a, b) = \Sigma(0, 1, 3)$ . (06 Marks)
- b. Realize the function  $T = f(w, x, y, z) = \Sigma(1, 3, 4, 6, 7, 9, 10, 13)$  using 8:1 Mux. (06 Marks)
- c. Design 2-bit binary comparator. (08 Marks)

OR

- 4 a. Realize Decimal to BCD priority encoder. (10 Marks)
- b. Realize the Boolean function  $F = f(a, b, c) = \Sigma(0, 2, 4, 5, 7)$  using 8:1 Mux. (10 Marks)

### Module-3

- 5 a. Explain the operation of SR-Flip-Flop with the help of functional table and logic diagram. (08 Marks)
- b. What is race-around condition? Explain with logic diagram. (06 Marks)
- c. Obtain the characteristic table and characteristic equation for JK-Flip-Flop. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Explain the working of Master – Slave JK Flip-Flop with the help of logic diagram. (08 Marks)
- b. Explain the working of positive edge triggered D-Flip-Flop with the help of logic symbol and function table. (08 Marks)
- c. Write the difference between latch and flip-flop. (04 Marks)

**Module-4**

- 7 a. What is register? Explain 4-bit serial-in serial-out unidirectional shift register with the help of diagram. (10 Marks)
- b. Explain 4-bit Asynchronous up and down counter. (10 Marks)

OR

- 8 a. Explain 3-bit up/down counter using mode-control input. (10 Marks)
- b. Design MOD-5 synchronous counter using JK-flip-flops. (10 Marks)

**Module-5**

- 9 a. What are Mealy and Moore models? Explain. (10 Marks)
- b. Design 2-bit synchronous counter. (10 Marks)

OR

- 10 a. Write state table and state diagram with an example. (10 Marks)
- b. Give Excitation table and equations for T-flip flop and explain the operation. (10 Marks)

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