CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, June/July 2023
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Simplify the following function using Quine McClusky method:
$P = f(w, x, y, z) = \Sigma(7, 9, 12, 13, 14, 15) + \Sigma d(4, 11)$ **(10 Marks)**

b. Write the truth table of the logic circuit having 4 inputs: A, B, C, D and an output Y.
$Y = f(A, B, C, D) = \overline{A}\,\overline{B}C\overline{D} + \overline{A}BC\overline{D} + AB\overline{C}\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}\overline{C}D + A\overline{B}CD$
Also simplify the Boolean expression and implement the logic circuit using NAND gates only. **(06 Marks)**

OR

2 a. Simplify the given function using MEV technique taking the least significant variable as the map entered variable.
$f(a, b, c, d, e) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25, 27, 28, 30) + \Sigma d(8, 10, 24, 26)$ **(08 Marks)**

b. Simplify the following function using K-map technique and implement using basic gates:
$f(A, B, C, D) = \pi M(0, 2, 4, 10, 11, 14, 15)$ **(08 Marks)**

Module-2

3 a. Distinguish between a decoder and an encoder implement full adder using IC74138. **(06 Marks)**

b. Write a short note on 4 bit parallel adder. **(04 Marks)**

c. Implement the following Boolean function using 4:1 multiplexer:
$Y = f(A, B, C, D) = \Sigma m(0, 1, 2, 4, 6, 9, 12, 14)$ **(06 Marks)**

OR

4 a. Explain the working of carry look ahead adder with the help of block diagram. **(06 Marks)**

b. Define multiplexer and demultiplexer. Draw the functional diagram. **(05 Marks)**

c. Design priority encoder with three inputs, with middle bit at highest priority encoding to 10, most significant bit at next priority encoding to 11 and least significant bit at least priority encoding to 01. **(05 Marks)**

Module-3

5 a. Explain the operation of master-slave JK flip flop with logic diagram, truth table, symbol and timing diagram. **(10 Marks)**

b. Obtain the characteristic equation of a SR flip flop. **(06 Marks)**

OR

6 a. Convert SR flipflop to a JK flipflop. **(06 Marks)**

b. Explain with the timing diagram the working of SR latch as a switch debouncer. **(10 Marks)**

Module-4

7 a. Construct the transition table, state table and state diagram for the Moore sequential circuit shown in the Fig.Q7(a).

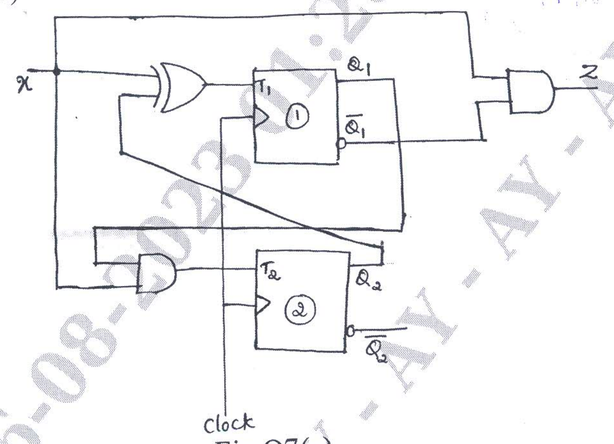

Fig.Q7(a) (10 Marks)

b. Explain Melay and Moore models of a clocked synchronous sequential circuit. (06 Marks)

OR

8 a. Design sequential circuit using JK flipflop. The state diagram shown in Fig.Q8(a).

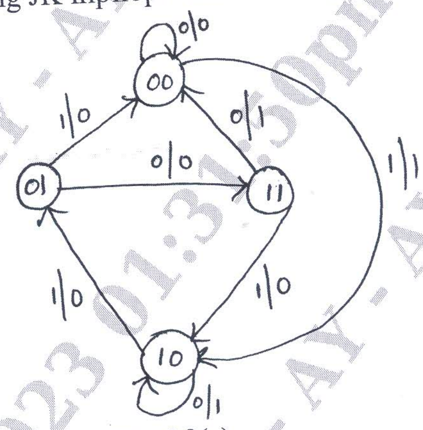

Fig.Q8(a) (12 Marks)

b. Define state, state equation, state diagram and state table. (04 Marks)

Module-5

9 a. Explain various data types available in VHDL. (10 Marks)
b. Implement a single bit comparator for all input combinations in VHDL. (06 Marks)

OR

10 a. Compare VHDL and Verilog. (10 Marks)
b. Implement a 4:1 multiplexer using a process and case statement in VHDL. (06 Marks)

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