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18EC753

Seventh Semester B.E. Degree Examination, June/July 2023
ARM Embedded System

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain pipeline mechanism for RISC processor to execute instructions. **(06 Marks)**

b. Illustrate with diagram the ARM-based embedded device, a micro controller. **(08 Marks)**

c. With the help of bit layout diagram, explain current program status register of ARM. **(06 Marks)**

OR

2 a. Describe the physical features that driven the ARM processor design. **(08 Marks)**

b. Outline boot code initialization process with four typical software components required to control an embedded device. **(08 Marks)**

c. List the applications of ARM processor. **(04 Marks)**

Module-2

3 a. Explain MSR and MRS instructions with syntax. **(08 Marks)**

b. Discuss load-store instruction with respect to single register transfer. **(08 Marks)**

c. With an example, explain SWAP instruction in ARM. **(04 Marks)**

OR

4 a. Categorize Logical and Arithmetic instructions used in ARM programming. **(07 Marks)**

b. Explain the operation of Barrel shifter with possible instructions. **(07 Marks)**

c. Write an ALP to find SUM of 8 integer numbers. **(06 Marks)**

Module-3

5 a. Discuss register usage in Thumb. **(06 Marks)**

b. Explain Thumb software Interrupt instruction with an example. **(06 Marks)**

c. Compare ARM and Thumb instructions and show that how Thumb instructions takes less memory than ARM instructions with an example code. **(08 Marks)**

OR

6 a. Explain ARM-Thumb interworking with example. **(06 Marks)**

b. Write an ALP to find the factorial of a number. **(06 Marks)**

c. Write description for the given Thumb mnemonics. SBC, CMN, BIC, ASR. **(08 Marks)**

Module-4

7 a. List the various issues that one may encounter when porting "C" code to ARM. **(05 Marks)**

b. Explain non-nested interrupt handler with related flow diagram. **(10 Marks)**

c. Mention various Interrupt handling schemes. **(05 Marks)**

OR

8 a. With neat diagram, explain processor exceptions and associated modes. **(07 Marks)**

b. Write code for enabling and disabling IRQ and FIQ interrupts. **(08 Marks)**

c. Brief about Link Register offsets. **(05 Marks)**

Module-5

9 a. Illustrate the relationship that cache has between processor core and main memory. **(10 Marks)**

b. Explain memory hierarchy with neat diagram. **(10 Marks)**

OR

10 a. With help of neat block diagram, differentiate between logical and physical caches. **(10 Marks)**

b. Write a note on firmware with firmwares execution flow. **(10 Marks)**

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