CBCS SCHEME

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17CS72

Seventh Semester B.E. Degree Examination, June/July 2023
Advanced Computer Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain with a neat diagram, the element of modern computer system. **(10 Marks)**
b. Briefly explain the architecture of vector super computer with a neat diagram. **(10 Marks)**

OR

2 a. With a diagram, explain the tagged token data flow computer. **(10 Marks)**
b. List out metrics affecting scalability of a computer system and briefly discuss the same. **(10 Marks)**

Module-2

3 a. Compare the CISC and RISC process architectures with neat diagram. **(10 Marks)**
b. Explain the architecture of VLIW processor and its pipeline system. **(10 Marks)**

OR

4 a. Explain Hierarchical memory technology with respect to inclusion, coherence and locality of references. **(10 Marks)**
b. Explain the address translation mechanism using TLB and various forms of page tables. **(10 Marks)**

Module-3

5 a. With diagrams, explain central bus arbitration and distributed bus arbitration. **(10 Marks)**
b. Explain Cache addressing models and direct mapping cache. **(10 Marks)**

OR

6 a. Briefly discuss sequential and weak consistency models with necessary schematic diagrams. **(10 Marks)**
b. Discuss static arithmetic pipelines and distinguish between an n-bit carry propagate adder (CPA) and an n-bit Carry – Save Adder (CSA). **(10 Marks)**

Module-4

7 a. Explain with schematic diagrams inter-process cross bar network design and a row of cross point switch design in a cross bar network. **(10 Marks)**
b. Explain Routing in Omega network. **(10 Marks)**

OR

8 a. Explain Snoopy bus protocol approach to ensure coherence. **(10 Marks)**
b. Discuss the three generation of multi-computers. **(10 Marks)**

Module-5

9 a. Explain Inter Process Communication (IPC) mechanisms using
i) Shared variable Model ii) Message passing Model. **(10 Marks)**
b. Explain different phases in optimizing compilers for parallelism. **(10 Marks)**

OR

10 a. Explain different language features for parallelism. **(10 Marks)**
b. Discuss the following (any two only)
i) Tomasulo's Algorithm ii) Reorder Buffer iii) Register Renaming **(10 Marks)**

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