USN

10CS74

Seventh Semester B.E. Degree Examination, June/July 2023
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: Answer any FIVE full questions, selecting at least TWO questions from each part.

PART – A

1 a. Discuss the three classes of computers with their characteristics. **(06 Marks)**

b. Define Amdahl's law. Derive an expression for CPU clock as a function of instruction count, clocks per instruction and clock cycle time. **(08 Marks)**

c. Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Suppose we have made the following measurements:
Frequency of FP operations = 25%
Average CPI of FP operations = 4.0
Average CPI of other instructions = 1.33
Frequency of FPSQR = 2%
CPI of FPSQR = 20
Compare these two design alternatives using processor performance equation. **(06 Marks)**

2 a. What is pipelining? List pipeline hazards. Explain any one in detail. **(10 Marks)**

b. With a neat diagram, explain the classic five stage pipeline for RISC processor. **(10 Marks)**

3 a. Explain the four methods for reducing pipeline branch penalties. **(08 Marks)**

b. What is data dependencies? Mention the different types of dependencies. Explain name dependencies with example between two instructions. **(06 Marks)**

c. What is correlating branch predictors? Explain with examples. **(06 Marks)**

4 a. With a neat diagram, explain the Intel Pentium 4 micro architecture. **(08 Marks)**

b. Write a note on branch target buffer. **(06 Marks)**

c. Mention the key issues in implementing advanced speculation techniques. Explain. **(06 Marks)**

PART – B

5 a. Explain the directory based cache coherence for a distributed memory multiprocessor system along with state transition diagram. **(10 Marks)**

b. Explain any two hardware primitives to implement synchronization, with example. **(10 Marks)**

6 a. Which are the basic cache optimization methods? Explain any two in detail. **(10 Marks)**

b. Assume we have a computer where the clocks per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? **(10 Marks)**

7 a. List and explain three C's model that sorts all cache misses. **(04 Marks)**

b. Explain the advanced optimization methods mentioned below:

(i) Trace cache to reduce hit time

(ii) Non-blocking cache to increase cache bandwidth

(iii) Multi banked cache to increase cache band width **(09 Marks)**

c. Briefly explain how memory protection is enforced via virtual memory. **(07 Marks)**

8 a. What do you mean by Loop Level Parallelism (LLP)? Explain with example. **(06 Marks)**

b. What is Global Code Scheduling? Explain with example. **(07 Marks)**

c. Explain Intel IA-64 architecture. **(07 Marks)**

* * * * *