CBCS SCHEME

USN | | | | | | | | | | |

18MT36

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the basic operational concept of a computer with neat diagram. **(08 Marks)**
b. Explain the different functional units of a digital computer. **(06 Marks)**
c. Write the basic performance equation. Explain the role of each of the parameters in the equation on the performance of the computer. **(06 Marks)**

OR

2 a. With relevant figure define the little endian and big-endian assignment. **(06 Marks)**
b. Classify basic instruction types with example. **(08 Marks)**
c. List the different system used to represent signed numbers perform the following operations on a 4bit signed number using 2's complement representation system i) $(+5) + (-2)$ ii) $(+2) - (-3)$. **(06 Marks)**

Module-2

3 a. Explain any five addressing modes with example. **(10 Marks)**
b. Explain briefly basic input/output operation. **(05Marks)**
c. What is stack? Write a routine for safe push operation and pop operation. **(05 Marks)**

OR

4 a. What are assembler directives? Explain assembler directives with example program. **(10 Marks)**
b. What is subroutine? Explain with diagram subroutine linkage using link register. **(05 Marks)**
c. Explain logical and arithmetic shift instruction. **(05 Marks)**

Module-3

5 a. Define memory mapped I/O and I/O mapped I/O with example. **(06 Marks)**
b. Discuss the different schemes available to enable and disable interrupts. **(06 Marks)**
c. What is interrupt? Explain transfer of control through the use of interrupt. **(08 Marks)**

OR

6 a. With neat diagram, explain use of DMA controllers in a computer system. **(10 Marks)**
b. Explain with diagram interrupt priority schemes. **(10 Marks)**

Module-4

7 a. Explain types of read only memory with diagram. **(10 Marks)**
b. Discuss internal organization of 2m * 8 dynamic memory chips. **(10 Marks)**

OR

8 a. Explain the memory hierarchy with neat diagram. **(10 Marks)**

b. Explain virtual memory organization with neat diagram. **(10 Marks)**

Module-5

9 a. Explain single bus organization of datapath with a neat block diagram. **(10 Marks)**

b. Explain with neat sketch hardwired control unit organization. **(06 Marks)**

c. Write a control sequence for execution of the instruction add R4, R5, R6 in three bus organization. **(04 Marks)**

OR

10 a. Write the control sequence for instruction execution for Add (R3), R1 in the execution of a complete instruction. **(10 Marks)**

b. Draw and explain multiple bus organization. **(10 Marks)**

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