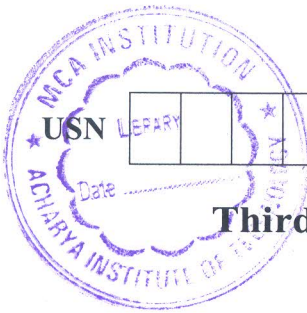


CBCS SCHEME

18MT35



Third Semester B.E. Degree Examination, Jan./Feb. 2023 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram, explain diode clippers, what is used to achieve clipping at two levels. (06 Marks)
- b. Explain with neat diagram, positive clamping circuit. (06 Marks)
- c. Explain with neat diagram, the working of RC coupled BJT amplifier. (08 Marks)

OR

- 2 a. Derive gain expression and explain with circuit diagram, first order high pass Butterworth filter. (10 Marks)
- b. Explain with neat diagram, the working principle of Narrow band reject filter. (10 Marks)

Module-2

- 3 a. State Barkhausen criterion for sustained oscillations and design phase shift oscillator for frequency 200Hz. (10 Marks)
- b. Design Weinbridge oscillator for frequency 965Hz given $C = 0.05\mu\text{f}$ and $R_1 = 12\text{K}\Omega$. (10 Marks)

OR

- 4 a. Explain the working of Schmitt trigger with necessary waveforms. (10 Marks)
- b. Explain with neat diagram comparator and its application. (10 Marks)

Module-3

- 5 a. Derive the expression for pulse width and explain the working of monostable multivibrator. (12 Marks)
- b. Explain monostable multivibrator as frequency divider. (08 Marks)

OR

- 6 a. Explain the operation of 555 timer as Astable multivibrator and derive an expression for duty cycle. (12 Marks)
- b. Explain Astable multivibrator as a square wave oscillator. (08 Marks)

Module-4

- 7 a. Using K-map solve
 - i) $V = f(w, x, y, z) = \sum(1, 7, 8, 9, 10, 11) + \sum d(5, 13, 15)$
 - ii) $T = f(w, x, y, z) = \pi(1, 3, 8, 10, 12, 13, 14, 15)$. (06 Marks)
- b. Implement $f(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$ using 8:1 mux. (06 Marks)
- c. Explain Quadruple 2 to 1 line multiplexer with common select and enable inputs. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 8 a. Design BCD to decimal decoder, using unused combinations of BCD code as don't care conditions. (12 Marks)
- b. With a logic diagram, explain octal to binary encoder. (08 Marks)

Module-5

- 9 a. With a neat circuit, analyze the operation of clocked RS flipflop and also derive characteristic equation from truth table. (10 Marks)
- b. Design 4-bit asynchronous ripple counter with logic and timing diagram. (10 Marks)

OR

- 10 a. Distinguish between:
- i) Combinational and sequential circuits (08 Marks)
 - ii) Synchronous and asynchronous counters.
- b. Design a mod-6 synchronous counter for sequence of $0 \rightarrow 2 \rightarrow 3 \rightarrow 1 \rightarrow 5 \rightarrow 6$ using JK flip flop and minimum gates. (12 Marks)
