# GBCS SCHEME

J. Committee	U.E. M.	and the			
	USN			18EC753	
	mate .	1 8 8 15 15 15 15 15 15 15 15 15 15 15 15 15	Seventh Semester B.E. Degree Examination, Jan./Fe	eb. 2023	
ARM Embedded Systems				A	
110	3 84	150			
	Tin	ie: 3	hrs.	Max. Marks: 100	
Notes Anguar and EIVE full avections aboasing ONE full avection from each was					
ice.		Note: Answer any FIVE full questions, choosing ONE full question from each module.			
ract			Module-1		
malp	1	a.	Illustrate on the major design rules of RISC philosophy.	(08 Marks)	
las		b.	With block diagram, demonstrate your understanding on AMBA bus p		
eatec			system.	(08 Marks) (04 Marks)	
be tr		c.	Explain the functionality of interrupt controllers in embedded system.	(04 Marks)	
will 1			OR		
50, 1	2	a.	With neat diagram of ARM core data flow model, explain the various		
 ≪			the signal flow.	(10 Marks)	
42+		b.	Illustrate how the pipeline mechanism speeds up the execution process i	in RISC processors. (05 Marks)	
n eg,		c.	Demonstrate the role of interrupt vector table in the execution of		
appeal to evaluator and /or equations written eg, $42+8=50$ , will be treated as malpractice.			Draw IVT.	(05 Marks)	
ns w					
atio	2		With a second for a lateral size the avarious instructions excitable in	ADM for arithmetic	
r eq	3	a.	With one example for each, explain the various instructions available in operations.	(10 Marks)	
10/p		b.	With suitable syntax and addressing modes, demonstrate how the	,	
or ar			instructions can transfer, multiple registers between memory and the	processor in a single	
luate			instruction.	(10 Marks)	
eva			OR		
al to	4	a.	Identify the instructions which are used to control the program s	tatus registers. With	
appe	-	a.	appropriate syntax and example line of code, explain the same.	(07 Marks)	
ion,		b.	Write an ALP to perform the addition of 2 numbers stored in register	ers and also store the	
ficat		et en	result in the register. Let one of the data be a left shifted by one.	(03 Marks)	
lenti		c.	Describe how stack operations are performed using ARM instruction.	ons. Mention address	
of ic			modes and briefly explain them. With pre and post values, write the of following instructions:	operation done by the	
aling of identification,			(i) STMFD SP!, {r <sub>1</sub> , r <sub>4</sub> }		

## Module-3

STMED SP!  $\{r_1, r_4\}$ 

(ii)

a. Write a Thumb code to find given 16 bit number is even or odd and count the number of bytes in it (code density). (07 Marks)
b. How do you link the ARM and Thumb Code together? Explain the process. (06 Marks)

c. How the single register transfer is done in ARM using thumb instruction set? (07 Marks)

(10 Marks)

#### OR

- 6 a. Which instruction causes software interrupts in thumb mode? How it is different from ARM equivalent instruction. (05 Marks)
  - b. Write the differences between ARM code and Thumb code. Also illustrate on the registers used by thumb state. (07 Marks)
  - c. Write an ALP to perform logical operations of DATA's (AND, OR, EXOR and NOT). Write the PRE and POST values of the register used. (08 Marks)

#### Module-4

- 7 a. List and briefly describe the basic C data types for ARM compilers. (04 Marks)
  - b. What is exception handling? Explain the mechanism which is adopted to handle the exceptions which occur simultaneously. Also indicate the reasons for these exceptions.

c. What is interrupt latency? How to minimize it? (08 Marks)
(08 Marks)

### OR

- 8 a. Describe the issues which may be encountered when porting C code to the ARM. (12 Marks)
  - b. With the general description, explain briefly the interrupt handling schemes. (08 Marks)

#### Module-5

- 9 a. Summerize the common execution flow of firmware implementation. (10 Marks)
  - b. Indicate the technologies included in the firmware package developed by ARM. Describe the features of it.

    (10 Marks)

#### OR

- 10 a. Describe the components of Embedded Operating System. (10 Marks)
  - b. Draw the diagram to show the memory hierarchy and the significance of various memory components in the hierarchy. (10 Marks)

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