CBCS SCHEME

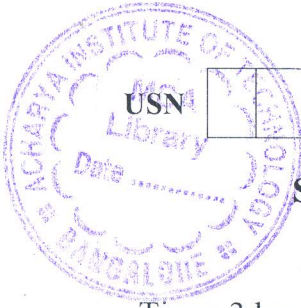15EC63

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
VLSI Design

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a.   With the help of diagrams, discuss various steps required to fabricate nMOS transistor.
         (08 Marks)
    b.   Discuss the working of nMOS transistor of enhancement type with the help of diagrams.
         (08 Marks)

OR

2   a.   Explain the CMOS inverter DC characteristics highlighting the regions of operation.
         (10 Marks)
    b.   Explain the following non-ideal effects for short channel MOSFETs :
         (i)   Body effect
         (ii)   Channel length modulation   **(06 Marks)**

Module-2

3   a.   Construct stick diagram and layout for the expression $f = \overline{A(B+C)}$ using nMOS design style.   **(10 Marks)**
    b.   Estimate nMOS inverter pair delay.   **(06 Marks)**

OR

4   a.   Derive an expression for rise time and fall time with respect to CMOS inverter.   **(08 Marks)**
    b.   Construct layout for the expression $f = \overline{AB + CD}$ using CMOS design style.   **(08 Marks)**

Module-3

5   a.   Discuss different bus architectures.   **(08 Marks)**
    b.   Discuss the design of 4 bit adder.   **(08 Marks)**

OR

6   a.   With relevant diagrams, discuss the operation of Manchester carry chain.   **(08 Marks)**
    b.   Analyze the operation of 4 bit carry look-ahead adder using multiple output domino logic.
         (08 Marks)

Module-4

7   a.   Discuss the operation of (n+1) lat parity generator with relevant circuit diagram and stick diagram.   **(10 Marks)**
    b.   Discuss the design of data selectors.   **(06 Marks)**

OR

8	a.	Explain the architecture of field programmable gate array.	(10 Marks)
	b.	Discuss the FPGA abstraction with diagram.	(06 Marks)

Module-5

9	a.	Explain three transistor DRAM with circuit diagram and stick diagram.	(08 Marks)
	b.	Explain the operation of D-latch using nMOS and CMOS.	(08 Marks)

OR

10	a.	Illustrate the operation of scan based testing using serial scan technique.	(08 Marks)
	b.	Explain the operation of Built In Logic Block Observation (BILBO) used in testing.	
			(08 Marks)

* * * * *