



CBCS SCHEME

17EC45

Fourth Semester B.E. Degree Examination, Jan./Feb. 2023 Linear Integrated Circuits

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain OFFSET voltages and currents of 741 op-amp. (06 Marks)
- b. Explain slew rate and frequency limitations with necessary diagrams. (08 Marks)
- c. Explain the method of OFFSET nulling with necessary circuit diagrams. (06 Marks)

OR

- 2 a. With neat circuit diagram, explain the circuit operation and design steps of direct coupled inverting amplifier. (08 Marks)
- b. Explain the circuit operation of the difference amplifier with necessary circuit diagrams and equations. (08 Marks)
- c. Explain the voltage follower compared with an emitter follower with neat circuit diagrams. (04 Marks)

Module-2

- 3 a. Design capacitor coupled voltage follower using 741 op-amp. The lower cut-off frequency for the circuit is 50 Hz and $R_L = 3.9 \text{ k}\Omega$. Given $I_{B_{\max}} = 500 \text{ nA}$, $R_L = 500 \Omega$ standard value. (07 Marks)
- b. Explain precision voltage source with neat circuit diagram. (05 Marks)
- c. Design an instrumentation amplifier to have an overall voltage gain of 900. The input signal amplitude is 15 mV. 741 op-amps are to be used. Supply is $\pm 15\text{V}$. Use $I_{B_{\max}} = 500\text{nA}$. (08 Marks)

OR

- 4 a. Explain the current amplifiers with neat circuit diagrams. (06 Marks)
- b. Explain the capacitor coupled voltage follower with neat circuit diagram and necessary equations. (08 Marks)
- c. Explain the setting procedure of upper cut-off frequency with neat circuit diagrams in 741 op-amp. (06 Marks)

Module-3

- 5 a. Design an adjustable peak clipping circuit to clip at approximately $\pm(3\text{V to }5\text{V})$. The circuit is to have unity voltage gain before clipping. ($I_{Z_{\min}} = 500 \mu\text{A}$). (06 Marks)
- b. Explain Dead Zone circuit with neat circuit diagram and waveforms. (06 Marks)
- c. A capacitor coupled zero crossing detector is to handle 1 kHz square wave input with peak to peak amplitude of 6V. Design suitable circuit using 741 op-amp with $\pm 12\text{V}$ supply. (08 Marks)

OR

- 6 a. Using 741 op-amp with supply of $\pm 12\text{V}$. Design an inverting Schmitt trigger circuit to have trigger points of $\pm 2\text{V}$. (07 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

- b. Explain the capacitor coupled crossing detector circuit with neat circuit diagram and waveforms. (07 Marks)
- c. Explain the precision clamping circuit with diagram and necessary equations. (06 Marks)

Module-4

- 7 a. Using 741 op-amp, design first-order active low pass filter to have cutoff frequency of 1 kHz. (07 Marks)
- b. Explain first order high-pass filter with neat circuit diagram and graph. (06 Marks)
- c. Design single stage bandpass filter to have voltage gain of 1 and passband from 300 Hz to 30 kHz ($C_2 = 1000 \text{ pF}$). (07 Marks)

OR

- 8 a. Explain fixed voltage series regulator and mention the characteristics of three terminal IC regulators. (09 Marks)
- b. Explain the series op-amp regulator with neat circuit diagram. (06 Marks)
- c. Explain the Bandpass and summing circuit as Band stop filter with neat block diagram and waveform. (05 Marks)

Module-5

- 9 a. Explain the basic block diagram of Phase-Locked Loop (PLL). (06 Marks)
- b. Find the output voltage by D/A converter whose output voltage range is 0 to 10V and whose input binary number is
 (i) 10 (For 2-bit D/A converter)
 (ii) 0110 (For 4-bit DAC)
 (iii) 10111100 (For 8-bit DAC) (07 Marks)
- c. Explain the Functional diagram of the successive approximation ADC. (07 Marks)

OR

- 10 a. Explain digital Exclusive-OR phase detector with necessary diagrams. (06 Marks)
- b. Explain the block diagram of voltage controlled oscillator with waveforms and equations. (08 Marks)
- c. Calculate the value of the LSB, MSB and Full scale output for an 8-bit DAC for the 0 to 10V range. (06 Marks)

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