CBCS SCHEME

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17EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Derive an expression to find the input impedance output impedance and voltage gain of a transistor connected in CE mode using voltage divider biasing. Use re model. **(08 Marks)**

b. For the circuit shown in Fig. Q1 (b) , find r_e, z_i, z_o and A_V and A_i with $r_o = \infty$. If r_o is changed to 50 kΩ, calculate z_i, A_V, A_i and Z_O and compare the results obtained with $r_o = \infty$. **(08 Marks)**

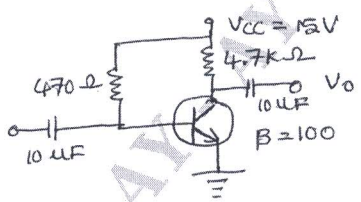


Fig. Q1 (b)

c. Mention the important characteristics of emitter follower. **(04 Marks)**

OR

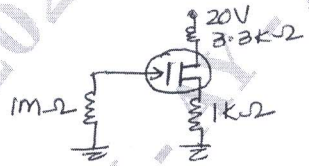
2 a. Draw the AC equivalent circuit of a emitter follower configuration and using approximate h-model find an expression to calculate the input impedance, output impedance, voltage gain and current gain. **(10 Marks)**

b. Find an expression to calculate the input impedance, voltage gain and output impedance of a transistor using complete hybrid model. **(10 Marks)**

Module-2

3 a. Compare BJT with FET. **(04 Marks)**

b. For the circuit shown in Fig. Q3 (b), calculate (i) V_{GSQ} (ii) I_{DQ} (iii) V_{DS} (iv) V_S (v) V_G and (vi) V_D. **(08 Marks)**



$V_{DSS} = 8$ mA
$V_P = -6$ V

Fig. Q3 (b)

c. Derive an expression to find the input impedance, output impedance and voltage gain of a n channel FET using common gate configuration. **(08 Marks)**

OR

4 a. Draw the construction of depletion type MOSFET and explain ion drain and transfer characteristic. **(08 Marks)**

b. Draw the ac equivalent circuit of JFET connected in common source configuration and find the expression to calculate input impedance, output impedance and voltage gain assume self bias. **(08 Marks)**

c. Sketch the small signal ac model of an FET and find the value of transconductance g_m and r_d if $Y_{fs} = 4$ mS and $Y_{OS} = 33.33$ μS. **(04 Marks)**

Module-3

5 a. Explain the low frequency response of BJT amplifier. **(10 Marks)**

b. Calculate the low frequency cut off for the network shown in Fig.Q5 (b) using the following values :

$C_G = 0.01\ \mu F$, $C_C = 0.5\ \mu F$, $C_S = 2\ \mu F$, $R_{sig} = 10\ K\Omega$, $R_G = 1\ M\Omega$, $R_D = 4.7\ K\Omega$, $R_S = 1\ K\Omega$, $R_L = 2.2\ K\Omega$, $I_{DSS} = 8\ mA$, $V_P = -4\ V$, $r_\phi = \infty$, $V_{DD} = 20\ V$. **(10 Marks)**

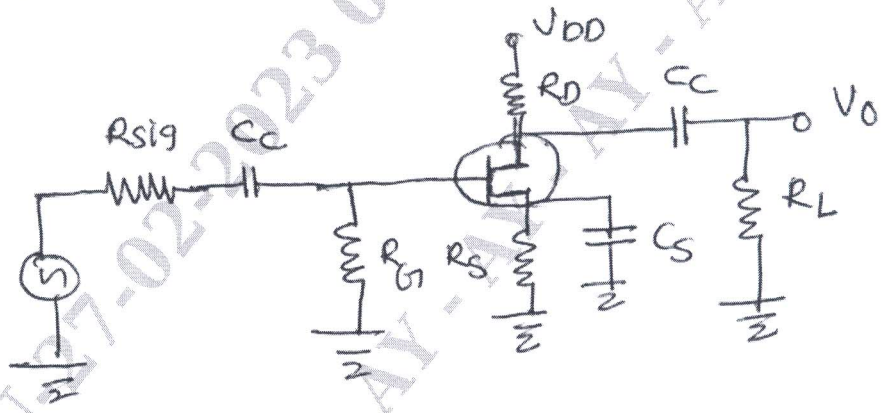


Fig. Q5 (b)

OR

6 a. What is Miller effect capacitance? Find an expression to calculate the input Miller capacitance and output Miller capacitance. **(10 Marks)**

b. Explain the high frequency response of an BJT amplifier. **(10 Marks)**

Module-4

7 a. Find an expression to calculate the input impedance, output impedance and voltage gain of current series feedback amplifier. **(08 Marks)**

b. An amplifier has a bandwidth of 200 kHz and voltage gain of 1000, find (i) the change in band width and gain if 5% negative feedback introduced (ii) to get a band width of 1 MHz, what is the amount of feedback required. **(08 Marks)**

c. Write the advantages of negative feedback. **(04 Marks)**

OR

8 a. Draw the circuit diagram of a weinbridge oscillator and explain its working. **(06 Marks)**

b. In a transistor Colpitts oscillator the inductor used is 1 mH and $h_{fe} = 150$. Find the value of C_1 and C_2 to produce oscillations of 120 kHz. **(06 Marks)**

c. Explain the working of UJT relaxation oscillator. **(08 Marks)**

Module-5

9 a. Explain how power amplifiers can be classified based on the location of Q point. **(04 Marks)**

b. Draw the circuit diagram of transformer coupled class A power amplifier and show the maximum conversion efficiency is equal to 50%. **(08 Marks)**

c. A Class B push pull amplifier is operated with $V_{CC} = 25\ V$ and $R_L = 8\ \Omega$, find (i) the maximum input power (ii) maximum output power and (iii) maximum circuit efficiency. **(08 Marks)**

OR

10 a. Draw the circuit of series voltage regulator using transistor and explain its operation. **(08 Marks)**

b. What is regulation and write the expression for voltage regulation. If a dc supply provides 50 V under no load condition and produces 46 V under load calculate the voltage regulation. **(06 Marks)**

c. Find the output voltage and zener current in regulator circuit shown in Fig. Q10 (c). **(06 Marks)**

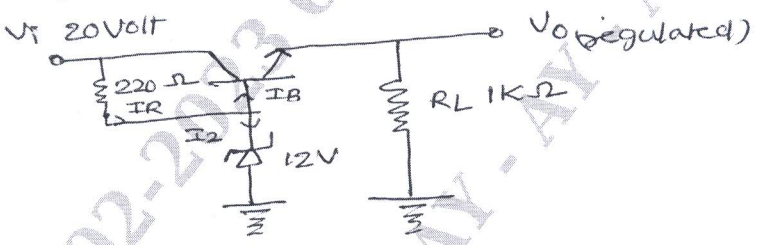


Fig. Q10 (c)

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