CBCS SCHEME

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18EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Convert the Boolean expression to canonical SOP form, $f = (xy + \bar{z})(y + x\bar{z})$. **(04 Marks)**

b. A switching circuit has four inputs A, B, C and D, and one output Y. The inputs A and B represent the bits of the number N_1, whereas the inputs C and D represent the bits of the number N_2. The output is to be high only if the product $N_1 \times N_2$ is less than 2. Draw the truth table and obtain the Maxterm expression. **(06 Marks)**

c. Simplify f(A, B, C, D, E) = Σ (5, 7, 9, 12, 13, 14, 15, 20, 21, 22, 23, 25, 29, 31) using a 5-varible K-map, and obtain the simplified SOP expression. **(10 Marks)**

OR

2 a. Convert the Boolean expression to canonical POS form $f = (a + b')(a + c)$. **(04 Marks)**

b. Use K-map to obtain the simplified POS expression for
$f(A, B, C, D) = (A + B + \bar{C})(\bar{B} + \bar{D})(\bar{A} + C)(B + C)$. **(06 Marks)**

c. Simplify f(a, b, c, d) = Σ(9, 12, 13, 15) + dΣ (1, 4, 5, 7, 8, 11, 14), using QM technique out of several possible solutions, select solution which can be implemented using only one AND gate and one OR gate. **(10 Marks)**

Module-2

3 a. Draw the circuit of 2 × 4 decoder having enable input and active high outputs. Give its truth table. **(04 Marks)**

b. Construct a 16 × 1 multiplexer using only 4 × 1 multiplexers. **(06 Marks)**

c. Four chairs A, B, C and D are placed in a row. When the chair is empty, it is logic – 0, and when the chair is occupied, it is logic – 1. Design and implement a circuit using 8 × 1 multiplexer IC such that, whenever the adjacent chairs are occupied, the output should go high. **(10 Marks)**

OR

4 a. Implement a single – bit binary comparator circuit using basic gates, and give its truth table. **(04 Marks)**

b. Implement the multiple output function using a single 3 × 8 decoder IC and additional gates. $f_1(a, b, c) = \Sigma(1, 4, 5, 7)$, $f_2(a, b, c) = \pi(2, 3, 6, 7)$. **(06 Marks)**

c. Derive the expressions and draw the complete logic circuit of a 4-bit look-ahead carry adder. **(10 Marks)**

Module-3

5 a. Draw the circuit of gated SR latch using NAND gates, and give its truth table. **(04 Marks)**

b. Construct a 4-bit parallel in serial out shift register using negative edge triggered D flip-flops. **(06 Marks)**

c. With neat diagram and truth table, explain the working of master slave JK flip-flop. The inputs shown in Fig Q5(c), are applied to the master slave JK flip-flop, which is initially in 0-state. Sketch the Q_M and Q_S outputs.

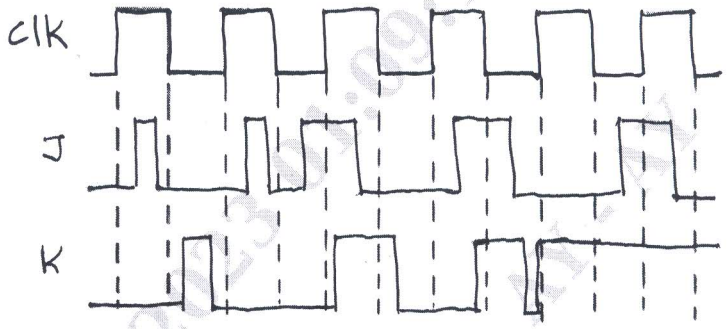

Fig Q5(c) **(10 Marks)**

OR

6 a. Give the comparison between combinational sequential circuits, with one example for each. **(04 Marks)**

b. Derive the characteristics equations of SR and JK flip-flops. **(06 Marks)**

c. Design a 4-bit binary ripple up-counter using positive edge triggered JK flip-flops. Neatly draw the timing diagrams, showing its complete count sequence. Mention the changes to be made in the above counter, using the same flip-flops so that it becomes a down-counter. **(10 Marks)**

Module-4

7 a. Draw the transition table and state diagram for the Moore circuit shown in Fig Q7(a).

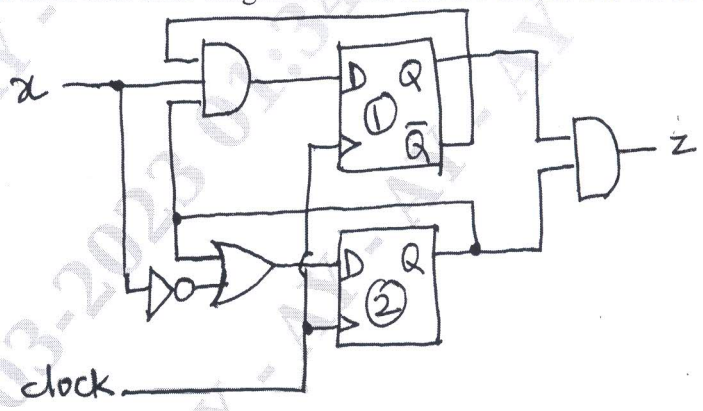

Fig Q7(a) **(08 Marks)**

b. Design a 3-bit synchronous counter having the repetitive count sequence of 0, 1, 2, 3, 5, 7 using JK flip flips. Check whether the counter is self correcting. **(12 Marks)**

OR

8 a. Design a mod – 5 synchronous binary counter, having the count sequence 0 to 4 and repeat, using D – flip-flops. **(08 Marks)**

b. Design a Mealy circuit for the state diagram shown in Fig Q8(b), Using JK flip-flops. Use the assignments: A = 00, B = 01 and C = 11.

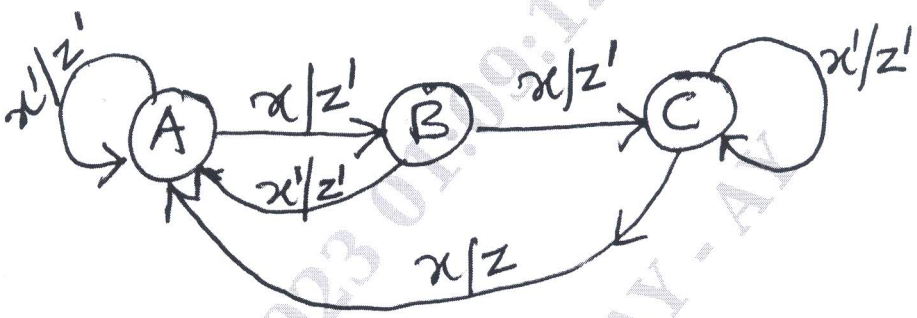

Fig Q8(b) **(12 Marks)**

Module-5

9 a. Construct a Mealy state diagram that will detect a serial input sequence of 10110 with overlap in a long data sequence. when the correct input pattern is detected, the output should go high. **(10 Marks)**

b. Design a Mealy state diagram for the sequential circuit that coverts a serial excess – 3 code to serial BCD code. The machine has to return to the beginning after four bits. The output should to high if the input is not a valid excess – 3 codes. **(10 Marks)**

OR

10 a. Draw the block diagram of a positive binary divider to divide an 8-bit dividend by a 4-bit divisor to obtain a 4-bit quotient and 4-bit remainder. Explain the operation briefly. **(10 Marks)**

b. Design a control circuit for a 4-bit serial adder using two shift register and a full adder. After receiving the start signal, the control circuit should give out four shift signals and then stop. When the addition is complete, the contents of one of the registers should be replaced by the sum. Draw the state diagram and transition table. Design and realize the circuit using D flip-flops. **(10 Marks)**

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