CBCS SCHEME

USN | | | | | | | | | | |

18EC33

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Electronic Devices

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the classification of material based on conductivity and energy band diagram. **(06 Marks)**

b. Explain with neat diagram direct and indirect semiconductors. **(08 Marks)**

c. Consider a semiconductor bar with $\omega = 0.1$ mm, $f = 10$ μm and $L = 5$ mm. For $\beta = 10$ kg ($1\ kg = 10^{-5}\ \omega b/cm^2$) and a current of 1 mA, we have $V_{AB} = -2$ mV and $V_{CD} = 100$ mV. Find the type, concentration and mobility of the majority carrier. **(06 Marks)**

OR

2 a. What is Hall effect? Explain with suitable diagram and equations how does Hall effect works? **(10 Marks)**

b. Compare between intrinsic and extrinsic material. **(06 Marks)**

c. Calculate the conductivity effective mass of electrons in silicon. (For silicon, $m_l = 0.98\ m_0$ and $m_t = 0.19\ m_0$) **(04 Marks)**

Module-2

3 a. Explain the qualitative description of current flow at p-n junction under equilibrium and biased condition. **(10 Marks)**

b. Explain zener break down and avalanche break down under reverse bias condition. **(10 Marks)**

OR

4 a. Explain photodetector in brief. **(08 Marks)**

b. Explain the piecewise linear approximation of junction diode under ideal condition. **(08 Marks)**

c. A silicon solar cell has a short circuit current of 100 mA and open circuit voltage of 0.8 V under full solar illumination. The fill factor is 0.7. What is the maximum power delivered to a load by this cell? **(04 Marks)**

Module-3

5 a. Draw Ebers-Moll model for a PNP transistor and explain its significance. **(10 Marks)**

b. With neat diagram, explain step by step fabrication of double poly silicon self aligned npn BJT. **(10 Marks)**

OR

6 a. Explain effect of base narrowing with neat diagram. **(06 Marks)**

b. Discuss switching operation in common emitter transistor. **(07 Marks)**

c. Explain with neat diagram the various components of current flow and current directions for normal active mode of operation of PNP transistor. **(07 Marks)**

Module-4

7	a.	Explain with neat diagram construction and operation of n-JFET.	(08 Marks)
	b.	Explain two terminal MOS structure using energy band diagram.	(08 Marks)
	c.	Explain n-channel enhancement mode MOSFET with its circuit symbol.	(04 Marks)

OR

8	a.	Draw and explain small signal equivalent circuit of n-channel PNJFET.	(07 Marks)
	b.	Explain with neat diagram ideal C-V characteristics of MOS capacitor with P-type substrate.	(07 Marks)
	c.	Explain the effect of frequency on gate voltage of a MOS capacitor with P-type substrate.	(06 Marks)

Module-5

9	a.	Explain low pressure conical vapour deposition reactors.	(07 Marks)
	b.	Explain photolithography process.	(07 Marks)
	c.	What are the advantages of integration?	(06 Marks)

OR

10	a.	Explain method of ION implantation with schematic diagram.	(10 Marks)
	b.	Explain integration of other circuit elements with suitable diagram.	(10 Marks)

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