CBCS SCHEME

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21EC32

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. What are combinational circuits? Give example. Explain combinational circuit with block diagram. **(04 Marks)**

b. Define canonical form representation and solve the following equation using canonical form
i) $P = f(a,b,c) = ab' + ac' + bc$
ii) $G = f(w,x,y,z) = w'x + yz'$. **(08 Marks)**

c. Simplify the following Boolean function using K – Map
i) $D = f(x, y, z) = \Sigma m(0, 2, 4, 6)$
ii) $K = f(a, b, c) = \Sigma m(1, 2, 3, 6, 7)$. **(08 Marks)**

OR

2 a. Define K-Map solve the following expression using K – Map.
i) $K = f(w, x, y, z) = \Sigma m(0, 1, 4, 5, 9, 11, 13, 15)$
ii) $D = f(a, b, c, d) = \Sigma m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. **(10 Marks)**

b. Define Quine-McClusky method and solve the following Boolean expression using Quine-McClusky method.
i) $D = f(a, b, c, d) = \Sigma m(0, 1, 2, 3, 6, 7, 8, 9, 14, 15)$
ii) $K = f(w, x, y, z) = \Sigma m(1, 3, 13, 15) + \Sigma d(8, 9, 10, 11)$. **(10 Marks)**

Module-2

3 a. Explain binary Adders with K–map and logical representation of equations for SUM and CARRY. **(06 Marks)**

b. Explain carry look ahead Adder with General and Sigma block. **(06 Marks)**

c. Explain working of decimal adder with neat block diagram (take example of BCD addition). **(08 Marks)**

OR

4 a. What are comparator circuits? Explain 2-bit magnitude comparators. **(08 Marks)**

b. Realize the Boolean expression using 3 : 8 decoder and two OR gates
i) $f_1(x_2, x_1, x_0) = \Sigma m(1, 2, 4, 5)$
ii) $f_2(x_2, x_1, x_0) = \Sigma m(1, 5, 7)$. **(06 Marks)**

c. Implement $D = (w, x, y, z) = \Sigma m(0, 1, 2, 4, 5, 7, 8, 9, 12, 13)$ using 8 : 1 MUX. **(06 Marks)**

Module-3

5 a. Write a note on Master Slave JK Flip-Flops with function table and timing diagram. **(08 Marks)**

b. What are Edge Triggered Flip-Flops. Explain positive edge Triggered and negative edge Triggered Flip-Flops. **(06 Marks)**

c. Write characteristic equation for : i) JK Flip-Flop ii) SR Flip-Flop. **(06 Marks)**

OR

6 a. Define Counters. Explain Binary Ripple counter with neat diagram. (08 Marks)
b. What are Registers? Explain any two classification registers with neat block diagram. (06 Marks)
c. Design synchronous MOD-6 counter using clocked JK Flip-Flops for sequences : 0 – 2 – 3 – 6 – 5 – 1. (06 Marks)

Module-4

7 a. Define HDL and types of HDL. Give structure of verilog module with example. (06 Marks)
b. Explain verilog logical operators with example. (06 Marks)
c. i) Write a note on verilog Data type
ii) Write verilog code for 8 × 1 MUX. (08 Marks)

OR

8 a. Give classification of Styles(Types) of description with example. (08 Marks)
b. Write verilog code for Full Adder. (06 Marks)
c. Write a note on Arithmetic and shift, Rotate relational operators with example. (06 Marks)

Module-5

9 a. Write a note on structure of Behavioural Description with example. (08 Marks)
b. Write a note on Signal Assignment and Variable Assignment with example. (06 Marks)
c. Write a note on sequential statement with example. (06 Marks)

OR

10 a. Write a verilog code for 2 × 1 MUX using if ELSE STATEMENT. (06 Marks)
b. Explain structural description with example. (08 Marks)
c. Explain structural description of 3-bit Ripple Carry Adder. (06 Marks)

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