CBCS SCHEME

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17EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Construct a truth table and write a Boolean expression for the problem statement: An output variable Y is true when the value of the inputs exceeds 3. Design the logic circuit for the obtained expression. **(10 Marks)**

b. What do you mean by canonical SOP a POS? Explain with an example. **(04 Marks)**

c. Simplify $s = f(a, b, c) = \sum m(0, 1, 3, 4, 5, 6)$ using K-map and draw the logic diagram using NAND gates for obtained expression. **(06 Marks)**

OR

2 a. Simplify using K-map method. $K = f(w, x, y, z) = \sum(0, 1, 3, 4, 5, 7, 9, 12, 13) + \sum d(2, 8, 10, 11, 14)$ and draw the logic circuit for obtained expression. **(10 Marks)**

b. Simplify using QM-method. $D = f(a, b, c, d) = \sum(0, 1, 2, 5, 7, 8, 9, 14, 15)$. Verify the same using K-map method. **(10 Marks)**

Module-2

3 a. Implement $f_1(a, b, c) = \sum(0, 2, 6)$ and $f_2(a, b, c) = \sum(1, 3, 7)$ using 74138, 3:8 decoder IC. **(06 Marks)**

b. With a neat circuit diagram, explain the carry look ahead adder with relevant expressions. **(06 Marks)**

c. Design 2-bit comparator using suitable gates. **(08 Marks)**

OR

4 a. Realize the function $y = f(a, b, c, d) = \sum(0, 1, 3, 5, 6, 7, 9, 10, 11, 13, 15)$ using 8:1 Mux. **(10 Marks)**

b. What is an Encoder? Design and explain 4:2 priority encoder. **(10 Marks)**

Module-3

5 a. Explain the working of Master-Slave JK-FF with the help of logic diagram. **(08 Marks)**

b. Obtain the characteristic equations for J-K and T-Flip-Flops (FF). **(06 Marks)**

c. What is race around condition and how it is overcome? Explain with the help of logic diagram. **(06 Marks)**

OR

6 a. Explain the working of gated SR-latch with the help of logic circuit. Draw the timing diagrams also. **(10 Marks)**

b. Explain the working of +ve edge triggered D-flip-flop with functional table. Draw the timing diagrams of the same. **(10 Marks)**

Module-4

7 a. Design 4-bit ripple up counter using positive edge triggered T-flip-flops and draw the truth table and timing diagram of the same. **(10 Marks)**

b. Explain the working of 4-bit of twisted ring counter with necessary logic diagram, truth table and timing diagrams. **(10 Marks)**

OR

8 a. What is register? Explain 4-bit serial-in, serial-out unidirectional shift register with the help of diagram. **(10 Marks)**

b. Design MOD-6 synchronous counter using SR flip-flops. **(10 Marks)**

Module-5

9 a. What are Mealy and Moore Models? Explain. **(08 Marks)**

b. Design 3-bit synchronous up counter. **(12 Marks)**

OR

10 a. Analyze the following sequential circuit of Fig.Q.10(a), by writing input and output equations, state table and state diagram. **(12 Marks)**

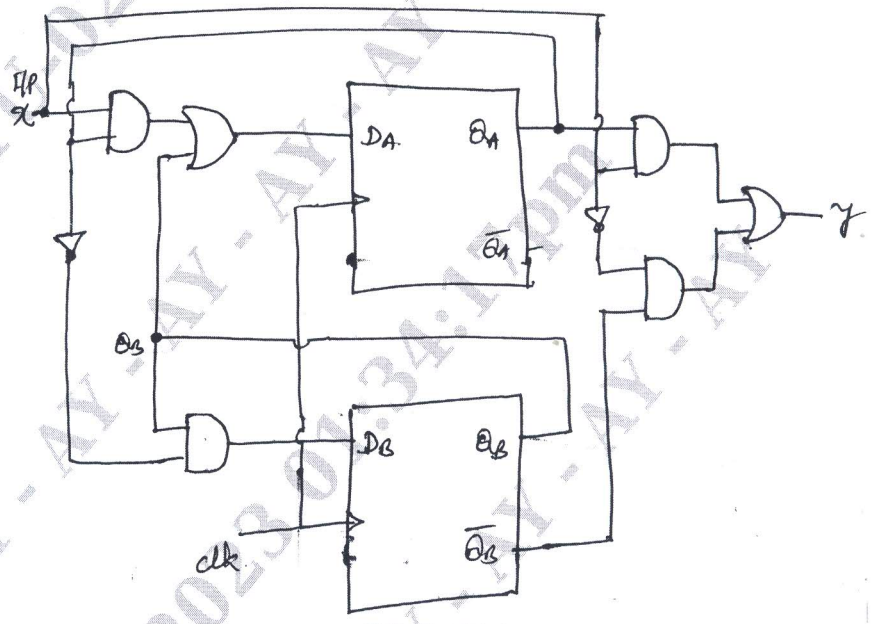

Fig.Q.10(a)

b. Draw a state table and state diagram with an example. **(08 Marks)**

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