CBCS SCHEME

USN | | | | | | | | | | |

15EE35

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: *Answer FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Show that $a'c + b'c' + ab = a'b' + bc + ac'$. **(06 Marks)**

b. The 4 inputs to a circuit (A, B, C, D) represent an 8 4 2 1 binary coded decimal digit. Design the circuit so that the output (z) is 1 if the decimal number represented by the inputs is exactly divisible by 3. Assume that only valid BCD digits occur as inputs. **(10 Marks)**

OR

2 a. Simplify the following expression using K-Map.
i) $f(A, B, C, D) = \pi M(0, 2, 3, 8, 9, 12, 13, 15)$
ii) $f(w, x, y, z) = \Sigma m(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$. **(08 Marks)**

b. Use Quine-McCluskey method and simplify the following function :
$f(a, b, c, d) = \Sigma m(0, 1, 2, 3, 8, 9)$. **(08 Marks)**

Module-2

3 a. Implement full subtractor using a decoder and write a truth table. **(06 Marks)**

b. Explain the design procedure for combinational circuits. **(06 Marks)**

c. Write short notes on Encoder. **(04 Marks)**

OR

4 a. Explain look ahead carry adder. **(10 Marks)**

b. Design 16 : 1 MUX using 8 : 1 MUX. **(06 Marks)**

Module-3

5 a. With a neat logic diagram explain working of a master slave JK flip-flop along with waveform. Also brief about race around condition. **(08 Marks)**

b. What is the difference between a flip-flop and a latch? With logic diagram and truth table, explain the operation of gated SR latch. **(08 Marks)**

OR

6 a. Convert D flip-flop to SR flip-flop. **(08 Marks)**

b. Design mod 6 ripple counter using T flip-flops. **(08 Marks)**

Module-4

7 a. With a suitable example, explain Mealy and Moore model in a sequential circuit analysis. **(08 Marks)**

b. Construct transition table, state table and state diagram for the given sequential circuit.

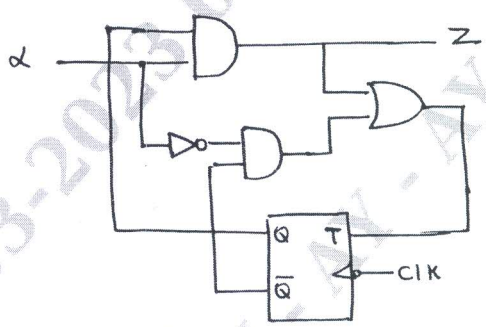

Fig.Q7(b) **(08 Marks)**

OR

8 a. Design synchronous mod 6 counter using D flip-flop to generate the sequence : (0, 2, 3, 6, 5, 1, 0 - - -). **(08 Marks)**

b. Describe the following terms with respect to sequential machines :
i) State
ii) Present state
iii) Next state
iv) State diagram. **(08 Marks)**

Module-5

9 a. Write the comparison between VHDL and verilog. **(08 Marks)**

b. Explain various data types available in VHDL.s **(08 Marks)**

OR

10 a. Explain the following :
i) Signal declaration and assignment statements
ii) Concurrent signal assignment statements. **(08 Marks)**

b. Explain shift and rotate operator in HDL with an example. **(08 Marks)**

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