CBCS SCHEME

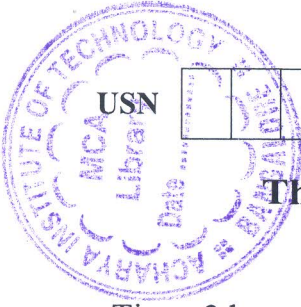USN [ ][ ][ ][ ][ ][ ][ ][ ][ ]   **18EE35**

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Digital System Design

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a.   A logic circuit has 4 inputs w, x, y, z and 2 outputs s_1 and s_2.
         (i) s_1 is '1' when majority of inputs are '1' (equal numbers of '0' and '1'are treated as don't core)
         (ii) s_2 is '1' when two adjacent inputs are '1'. (w and s are treated adjacent).
         Design the circuit using NAND gates only.   **(12 Marks)**

    b.   Find the minimal SOP and POS expressions of in completely specified Boolean function using K-map.
         (i) $f(a, b, c, d) = \Sigma m(6, 7, 9, 10, 13) + \Sigma d(1, 4, 5, 11, 15)$
         (ii) $f(a, b, c, d) = \pi m(1, 2, 3, 4, 9, 10) + \pi d(0, 14, 15)$ **(08 Marks)**

OR

2   a.   Express the following functions into their proper canonical form in decimal notation.
         (i) $M = P(\overline{q} + s)$ (ii) $N = (\overline{w} + x)(y + z)$ **(06 Marks)**

    b.   Simply the following function using Quine - McClusky method and realize the simplified expression using NOR gates.
         $w = f(A, B, C, D) = \Sigma m(7, 9, 12, 13, 14, 15) + \Sigma d(4, 11)$ **(14 Marks)**

Module-2

3   a.   Define magnitude comparator. Design a two-bit binary comparator and implement with suitable logic gates.   **(10 Marks)**

    b.   Implement the multiple functions using IC 74 LS138 and external gates.
         $F_1(A, B, C) = \Sigma m(1, 6, 7)$
         $F_2(A, B, C) = \pi M(0, 1, 2, 7)$ **(06 Marks)**

    c.   Define Demux. Design 1-4 Demux.   **(04 Marks)**

OR

4   a.   Implement $f(A, B, C, D) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$ using
         (i) 74151 (8-1 MUX)   (ii) 74153 (dual 4-1 MUX), A, B, C as select lines.   **(06 Marks)**

    b.   Explain the design of a carry look-ahead adder with a neat circuit diagram.   **(08 Marks)**

    c.   Design a 4 to 2 line priority encoder with valid output, where the highest priority is given to the highest bit position or input with highest index and obtain minimal sum expressions for the outputs.   **(06 Marks)**

Module-3

5   a.   Discuss the difference between a flip – flop and latch. Explain the operation of gates SR latch with a logic diagram truth table and logic symbol.   **(08 Marks)**

    b.   Explain the working of Master – Slave J-K flip-flops with functional table and timing diagram. Show how race around condition is overcome.   **(12 Marks)**

OR

6 a. Explain with timing diagram, the working of S.R latch as a switch debouncer. **(08 Marks)**
   b. Derive the characteristic equations for SR, JK, D and T flip-flop. **(08 Marks)**
   c. Explain the operation of basic bistable element using two inverter configuration. **(04 Marks)**

Module-4

7 a. Differentiate Synchronous and Asynchronous counter. **(04 Marks)**
   b. Explain the operation of a 4 bit ring and Jonson counter. **(08 Marks)**
   c. Design mod-6 synchronous counter using clocked J-K flip-flop for the given sequence $0 - 1 - 2 - 3 - 4 - 5 - 0$ **(08 Marks)**

OR

8 a. Explain the four modes of operation of a universal shift register with suitable logic diagram and truth table. **(12 Marks)**
   b. Design 4-bit binary ripple up – counter using positive edge T-flip flop. Write the counting sequence and draw timing diagram. **(08 Marks)**

Module-5

9 a. Explain Mealy model and Moore model in detail with necessary block diagram. **(08 Marks)**
   b. Analyse the following sequential circuit shown in Fig.Q9(b) and obtain the excitation, transition and state tables. Also draw the state diagram.

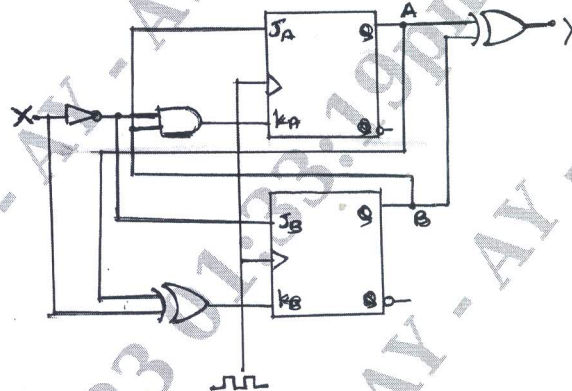Fig.Q9(b) **(12 Marks)**

OR

10 a. Design a clocked sequential circuit that operates as per the state diagram given in Fig.Q10(a), using D flip-flop.
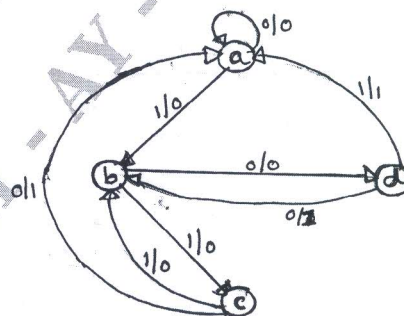

Fig.Q10(a) **(12 Marks)**

   b. Write a short note on :
      (i) ROM   (ii) RAM   (iii) EPROM   (iv) Flash Memory **(08 Marks)**

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