CBCS SCHEME

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15EE34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define clipping and clamping circuits. Explain type of clamping circuits. **(08 Marks)**

b. What is biasing of a transistor? Explain the factors that affect selection of Q-pt anywhere in the active region for the transistor to operate as an amplifier. **(08 Marks)**

OR

2 a. Derive the expression for stability factors for fixed bias circuit with respect to I_{CO}, V_{BE} and β. **(08 Marks)**

b. Define fixed bias circuit and explain with neat diagram. **(08 Marks)**

Module-2

3 a. State and prove Miller's theorem. **(04 Marks)**

b. Calculate the overall lower 3db and upper 3db frequency for a 3 stage amplifier having an individual frequency $f_i = 40hz$ and $f_2 = 2MHz$. **(04 Marks)**

c. Derive the expression for Miller's effect capacitances. **(08 Marks)**

OR

4 a. Define h-parameters and hence derive h-parameter model of a CE-BJT. **(08 Marks)**

b. A voltage source of negligible internal resistance drives a common collector transistor amplifier. The load resistance is 2500Ω. The transistor h-parameters are $h_{ie} = 1000\Omega$, $h_{re} = 1$, $h_{fe} = -50$ and $h_{oe} = 25\mu A/V$, compute A_i, A_v, Z_i and Z_0. **(08 Marks)**

Module-3

5 a. Explain the need of cascading amplifier, 'Draw and explain the Block diagram of two stage cascade amplifier. **(08 Marks)**

b. With block diagram, explain the concept of feedback amplifier. **(08 Marks)**

OR

6 a. List general characteristics of negative feedback amplifier. **(04 Marks)**

b. Determine the voltage gain input and output independence with feedback for voltage series having $A = -100$, $R_i = 10K\Omega$ and $R0 = 20K\Omega$ for feedback $\beta = -0.1$. **(06 Marks)**

c. A 2-stage cascade amplifier system is built with stage voltage gains 25 and 40. Both stages have the same bandwidth of 220KHz with identical lower cutoff frequency of 500Hz. Find the overall gain bandwidth product. **(06 Marks)**

Module-4

7 a. With a neat diagram, explain the working of a complementary symmetry class-B amplifier. **(08 Marks)**

b. A class – B push pull amplifier operating with V_{CC} = 25V provides a 22V peak signal to an 8Ω load. Find peak load cement, dc current drawn from the supply, input power, output power, circuit efficiency, power dissipation. **(08 Marks)**

OR

8 a. A crystal has the following parameter L = 0.3344, CM = 1pF, C = 0.065pF and R = 5.5kΩ. Calculate the series Resonant frequency, parallel resonant frequency and find the Q- of the crystal. **(08 Marks)**

b. With a neat diagram, explain RC phase shaft oscillator and write differentiate between RC phase shaft oscillator and wein bridge oscillator. **(08 Marks)**

Module-5

9 a. Draw the JFET amplifier using fixed bias configuration. Derive Z_i, Z_0 A_V using small signal nodel. **(08 Marks)**

b. Determine V_{GSQ} ,T_{DQ} and V_{DS}, V_D for circuit shown in Fig. Q9(b).

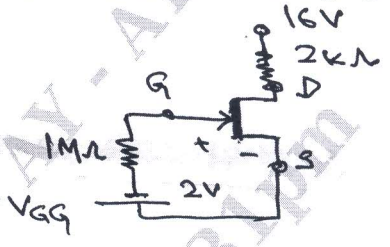


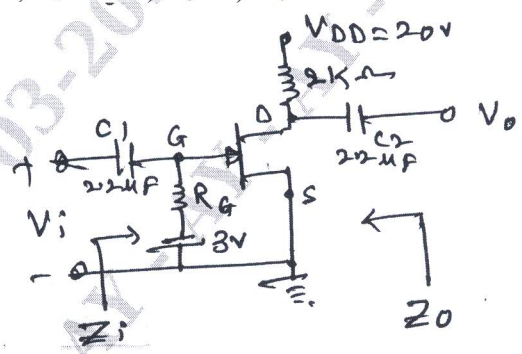
Fig. Q9(b) **(08 Marks)**

OR

10 a. Compare FET over BJT. **(04 Marks)**

b. With necessary equivalent circuit obtain the expression for Z_i and A_V for a JFET. Common gate configuration. **(06 Marks)**

c. For the JFET amplifier shown in below Fig Q10(c). Calculate:
i) g_m ii) r_d iii) Z_i iv) Z_0 v) A_v.



I_{DSS} = 5mA
V_P = -6V
Y_{DS} = 40μs
V_{GSQ} = -3V
R_G = 2mΩ

Fig Q10(c)

(06 Marks)

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