CBCS SCHEME

USN | | | | | | | | | | |

17CS44

Fourth Semester B.E. Degree Examination, Jan./Feb. 2023
Microprocessors and Microcontrollers

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain in detail about Execution unit and Bus interface unit of 8086 microprocessor, with neat diagram. **(08 Marks)**

b. With neat description of flag register explain about various flag bits of 8086 processor using suitable examples. **(06 Marks)**

c. Compute the physical address and logical address of destination operand and the contents of memory locations in each of the following addressing examples:
Assume the registers have following contents CS = 1000H, DS = 2008H, SS = 3800H, SI = 4000H, DI = 5000H, BX = 6080H, BP = 7020H, AX = 25FFH.
i) MOV[SI], AL ii) MOV[BX + 8], AH iii) MOV[BP] + 200, AX. **(06 Marks)**

OR

2 a. Discuss the following addressing modes with examples:
i) Direct ii) Immediate iii) Register Indirect iv) Indexed relative addressing mode. **(08 Marks)**

b. Differentiate between short, near and far jump instructions with example of each. **(04 Marks)**

c. What do you mean by segment override prefix? Explain the following assembler directives:
i) DQ ii) SMALL iii) PROC iv) EQU. **(08 Marks)**

Module-2

3 a. Explain the following instructions along with suitable examples: i) SBB ii) MUL iii) DAA iv) JA v) CMP. **(10 Marks)**

b. Explain with code snippet about how value of a given number 29 from standard input device is converted to its packed BCD conversion. **(06 Marks)**

c. Compute the value of BH register after executing the following instruction if BH = 42H and initial carry value is 1. i) ROR BH, 2 ii) RCR BH, 2. **(04 Marks)**

OR

4 a. Explain how the X86 PC executes interrupts by using the interrupt vector table and interrupt routines. **(06 Marks)**

b. Write an ALP to perform the following task:
i) Clear the screen
ii) Set the cursor at row 8 and column 5 of the screen
iii) Display the message "welcome". **(08 Marks)**

c. Explain about functionality of any 3 different options of int 21H. **(06 Marks)**

Module-3

5 a. With a neat diagram, explain NAND gate address decoder with starting address C000H for 128K * 8 memory chip and compute the address range. **(08 Marks)**

b. With an example explain about XLAT instruction. **(05 Marks)**

c. Write an assembly language program to reverse a given string and verify whether it is a palindrome or note and display appropriate message. **(07 Marks)**

OR

6 a. Explain about control word register of 8255 with neat diagram. Design and develop an ALP to demonstrate the BCD up counter (00 – 99) on device interface with all port as output. **(10 Marks)**

b. Assume that we have 5 bytes of data: 27H, 68H, 12H, 45H, 78H.

i) Find the checksum byte.

ii) Perform the checksum operation to ensure the data integrity.

iii) If 3rd byte is changed to 22H, show how checksum detects error. **(06 Marks)**

c. Write a note of SAR instruction with an example. **(04 Marks)**

Module-4

7 a. With neat diagram, explain about ARM based embedded device. **(07 Marks)**

b. Briefly explain the seven basic operating modes of ARM core with relevant diagram of various registers used in each mode. **(08 Marks)**

c. With a neat diagram, explain the CPSR register in detail. **(05 Marks)**

OR

8 a. With a neat diagram, explain about ARM core dataflow model. **(07 Marks)**

b. Explain about Von Neumann architecture with cache and Harvard architecture with tightly coupled memory core extensions to Arm processors. **(08 Marks)**

c. Discuss about the pipeline design for ARM9 family processor. **(05 Marks)**

Module-5

9 a. Explain the following instructions for ARM processor with an example:
i) RSC with C = 1 ii) MLA iii) BL iv) CMN v) SMULL. **(10 Marks)**

b. Explain the concept of Barrel shifter with ALU of ARM processor with

i) Mov r7, r5, LSR #2 with r5 = 8, r7 = 5.

ii) Mov r6, r4, LSL #2 with r6 = 8, r4 = 5. **(10 Marks)**

OR

10 a. Explain about MRS and MSR instruction with syntax and example. **(06 Marks)**

b. Discuss about software interrupt instruction. **(04 Marks)**

c. Explain about single register load-store addressing modes:

i) Preindex with immediate offset

ii) Immediate post indexed

iii) Scaled register post index

iv) Preindex with scaled register offset

v) Preindex write back register offset. **(10 Marks)**

* * * * *