CBCS SCHEME

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17MT36

ACHARYA INSTITUTE OF MCA Library Date ... BANGALORE

Third Semester B.E. Degree Examination, July/August 2022
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the different functional units of computer with a neat block diagram. **(10 Marks)**
b. Illustrate memory locations and addresses with necessary diagrams. **(10 Marks)**

OR

2 a. Explain with a neat diagram, the connection between processor and computer memory and also typical operation steps for executing an instruction. **(10 Marks)**
b. What are the basic instruction types? Explain. **(10 Marks)**

Module-2

3 a. Define addressing mode. Explain any three addressing mode with example. **(10 Marks)**
b. Discuss various logical shift and rotate instructions with example. **(10 Marks)**

OR

4 a. What are assembler directives? Explain with example. **(10 Marks)**
b. Explain the IEEE standard for floating point numbers. **(10 Marks)**

Module-3

5 a. What is DMA approach explain in detail. **(10 Marks)**
b. Explain how simultaneous interrupt requests from several I/O devices will be handled by a daily chain arrangement. **(10 Marks)**

OR

6 a. Explain standard I/O interfaces with an example of a computer using different interface standards. **(10 Marks)**
b. Explain the interface circuit of a serial port. **(10 Marks)**

Module-4

7 a. What is ROM? Explain various types of ROM. **(10 Marks)**
b. Explain direct mapped cache and associative mapped cache with neat block diagrams. **(10 Marks)**

OR

8 a. Draw the organization of 1K × 1 memory chip and explain its working. **(10 Marks)**
b. Explain synchronous DRAM operation with a neat block diagram. **(10 Marks)**

Module-5

9 a. Draw and explain the single bus organization of the data path inside a processor. **(10 Marks)**
b. Discuss the basic organization of a micro programmed control unit with a neat diagram. **(10 Marks)**

OR

10 a. Explain the three bus organization of a processor with a neat diagram. **(10 Marks)**
b. Give a detailed diagram of a hardwired control unit and explain its organization. **(10 Marks)**

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